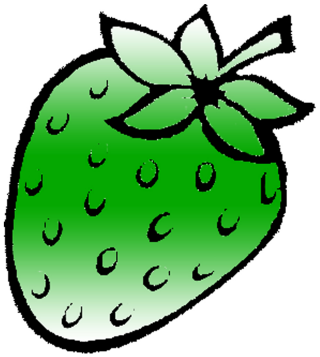
# STRAWBERRY



/strawberrydevelopers

/strawberry_app

For more visit:

Strawberrydevelopers.weebly.com

# FET ( Field Effect Transistor)

# Contents

- Junction FET
- Symbol
- Input/Output Characteristic
- Parameters
- JFET Biasing Methods

# Contents (Contd.)

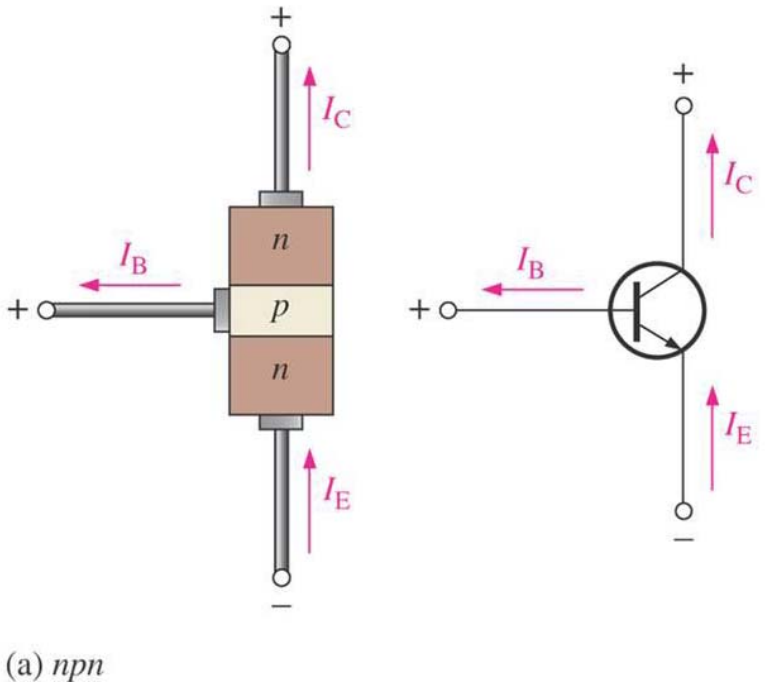
- MOSFET
- Symbol
- Input/Output Characteristic
- Parameters
- MOSFET Biasing Methods
- Applications – Switch, Digital Logic Gate and Amplifier.
- Temperature effects in MOSFETS
- Input Protection in MOSFET
- The Power FET (VMOS)

# Introduction

1. Field effect transistors control current by voltage applied to the gate.
2. The FET's major advantage over the BJT is high input resistance (typically many megaohms).
3. It is simpler to fabricate and occupies less space than bipolar transistor
4. It is less noisy than BJT.
5. Its operation depends on the flow of majority charge carriers only (unipolar).
6. Overall, the purpose of the FET is the same as that of the BJT.

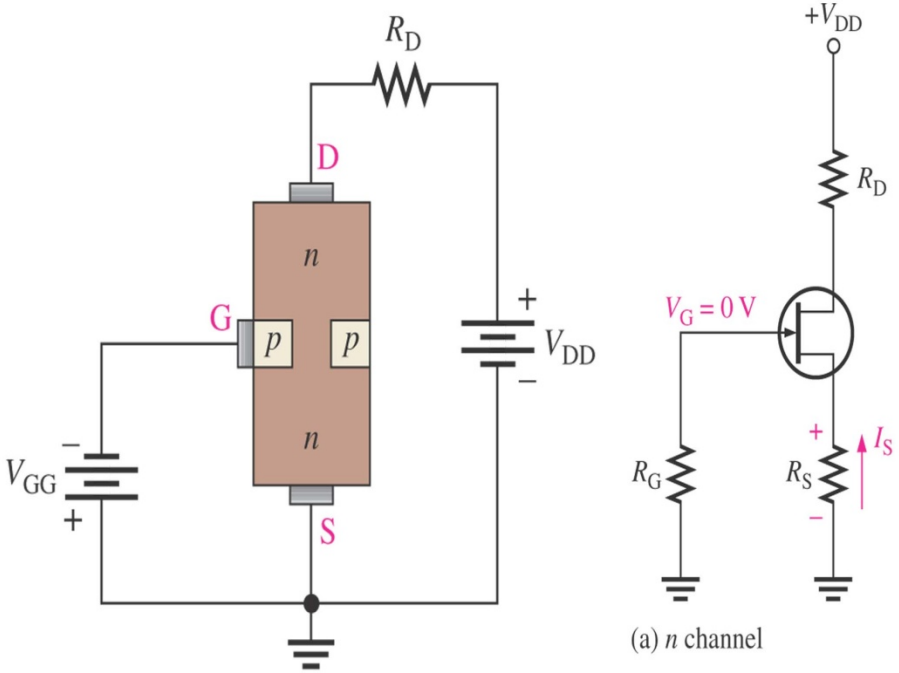
# BJT vs JFET

## BipolarJunctionTransistor




- Current-based device
- $I_{Base}$ controls $I_{CollectorEmitter}$

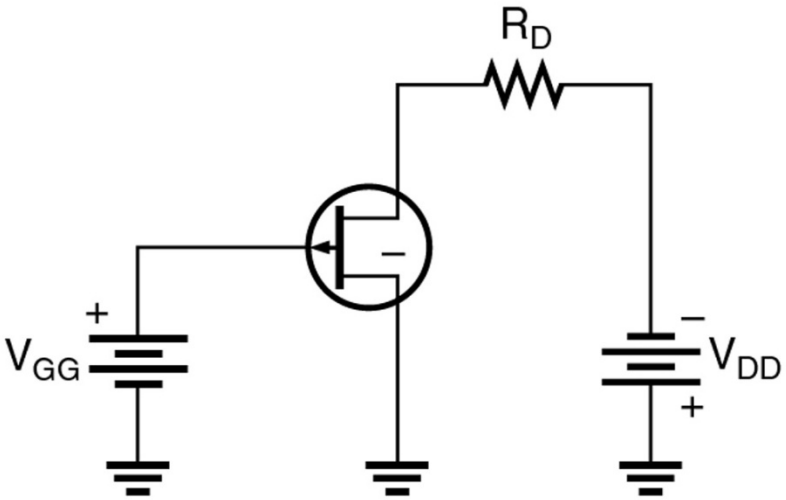
## JunctionFieldEffectTransistor




- Current-based device
- $V_{Gate}$ controls $I_{SourceDrain}$

# The JFET – Primary Characteristics

- Junction field effect transistor controls current flow.
- The JFET uses voltage to control the current flow.
- You will recall, the transistor uses current flow through the base-emitter junction to control current.
- JFETs can be used as an amplifier just like the BJT.




- $V_{GG}$ voltage level controls current flow in the VDD, $R_D$ circuit.

# The Field Effect Transistor (FET)

- The FET was known as a "unipolar" transistor.
- The term refers to the fact that current is transported by carriers of one polarity (majority), whereas in the conventional bipolar transistor carriers of both polarities (majority and minority) are involved.

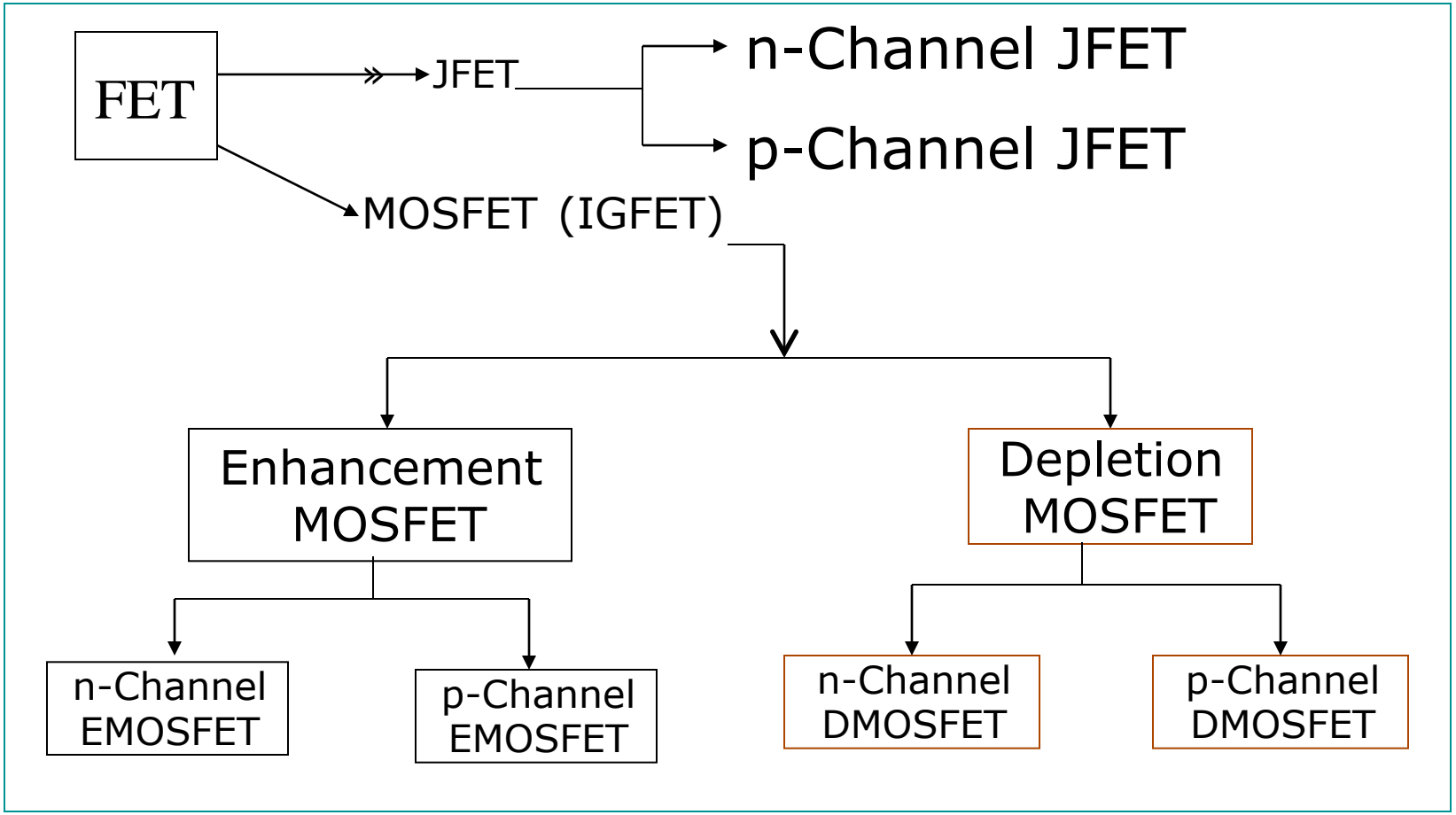
**Field-effect transistors** are so named because a weak electrical signal coming in through one electrode creates an electrical field through the rest of the transistor.

# Few important advantages of

# FET over conventional Transistors

1. Unipolar device i. e. operation depends on only one type of charge carriers (*h* or *e)* (MAJORITY CHARGE CARRIERS)
2. Voltage controlled Device (gate voltage controls drain current)
3. Very high input impedance ($\approx 10^9$-$10^{12}\ \Omega$)
4. Source and drain are interchangeable in most Low-frequency applications
5. Low Voltage Low Current Operation is possible (Low-power consumption)
6. Less Noisy as Compared to BJT
7. No minority carrier storage (Turn off is faster)
8. Self limiting device
9. Very small in size, occupies very small space in ICs
10. Low voltage low current operation is possible in MOSFETS
11. Zero temperature drift of out put is possible.

# Types of Field Effect Transistors (The Classification)



# The Field Effect Transistor (FET)

The family of FET devices may be divided into :

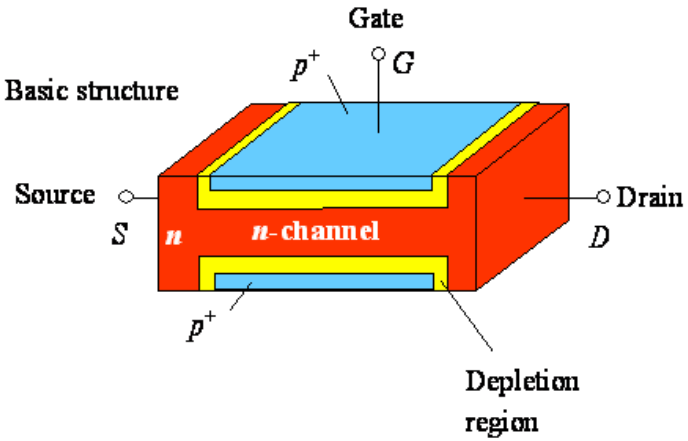
- Junction FET
- Depletion Mode MOSFET
- Enhancement Mode MOSFET

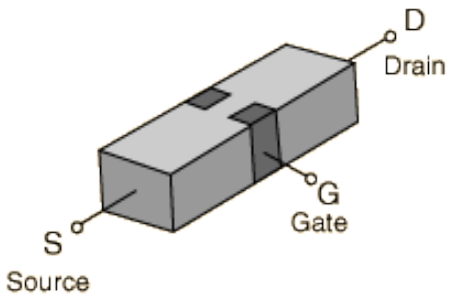
# Structure of

# The Junction Field Effect Transistor (JFET)

# Basic structure of JFETs

- JFETs consists of a piece of high-resistivity semiconductor material (usually Si) which constitutes a channel for the majority carrier flow.
- Conducting semiconductor channel between two ohmic contacts – source & drain



# N channel Junction Field Effect Transistor (JFET)

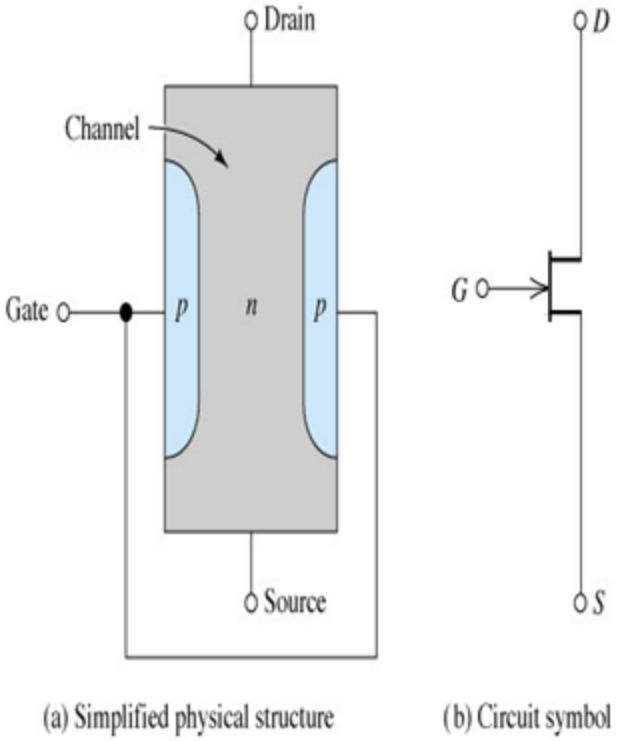



**Figure:** *n*-Channel JFET.

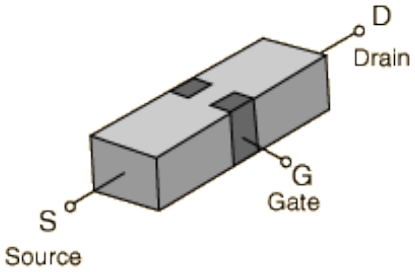
- The magnitude of this current is controlled by a voltage applied to a gate, which is a reverse-biased.
- The fundamental difference between JFET and BJT devices: when the JFET junction is reverse-biased the gate current is practically zero, whereas the base current of the BJT is always some value greater than zero.

# Basic structure of JFETs

- JFET is a high-input resistance device, while the BJT is comparatively low.
- If the channel is doped with a donor impurity, n-type material is formed and the channel current will consist of electrons.
- If the channel is doped with an acceptor impurity, p-type material will be formed and the channel current will consist of holes.
- N-channel devices have greater conductivity than p-channel types, since electrons have higher mobility than do holes; thus n-channel JFETs are approximately twice as efficient conductors compared to their p-channel counterparts.

# Basic structure of JFETs

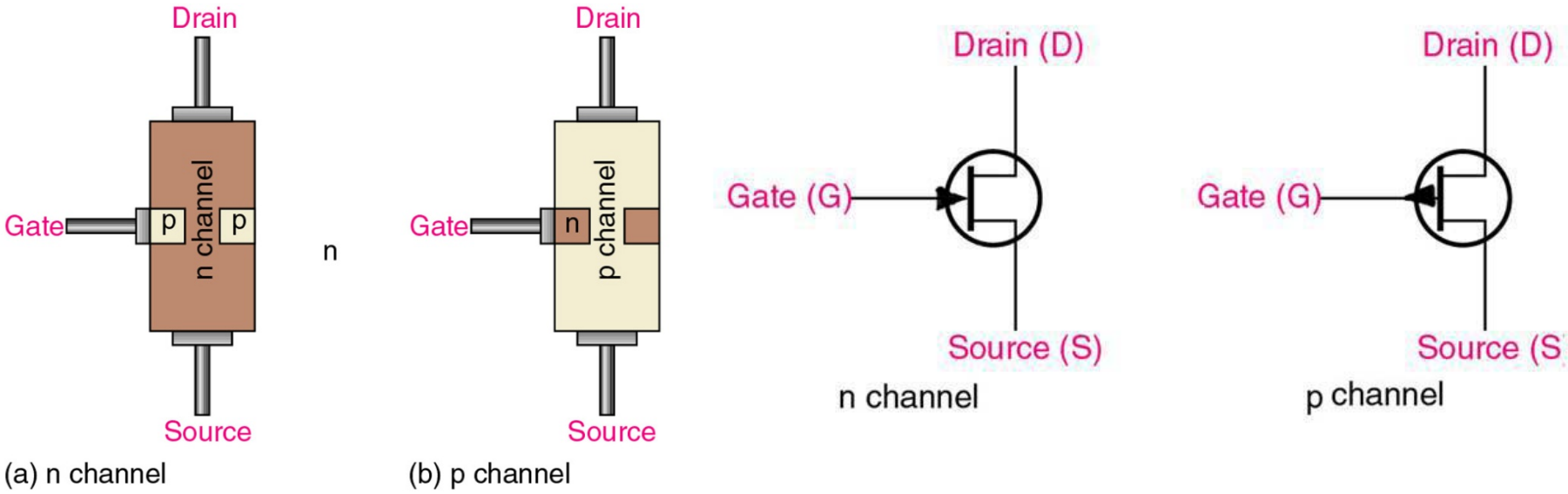
- In addition to the channel, a JFET contains two ohmic contacts: the source and the drain.
- The JFET will conduct current equally well in either direction and the source and drain leads are usually interchangeable.



# The JFET - Labels

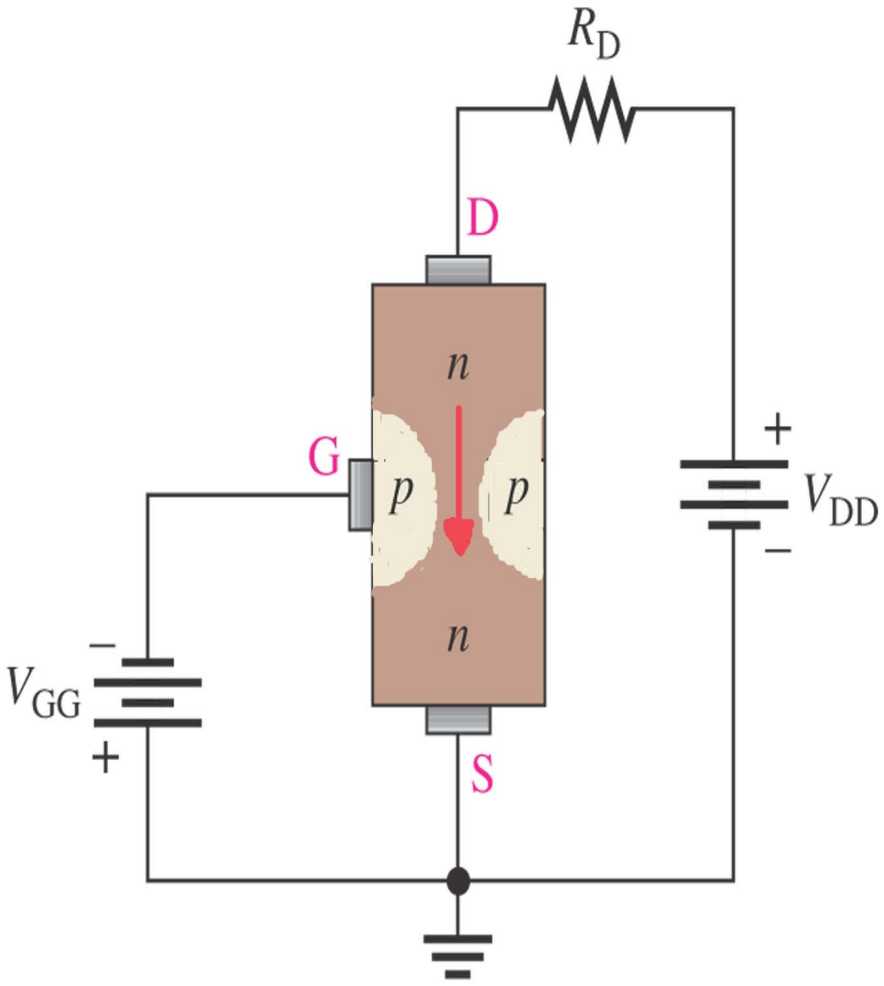
The terminals of a JFET are the source, gate, and drain.

A JFET can be either p channel or n channel.



# The JFET - Biasing

- The "source-drain" current is controlled by a voltage field at the "gate".
- That field is developed by the reverse biased gate-source junction (gate is connected to both sides).
- With more $V_{GG}$ (reverse bias) the field grows larger.
- This field or resistance limits the amount of current flow through $R_D$.
- With low or no $V_{GG}$ current flow is at maximum.

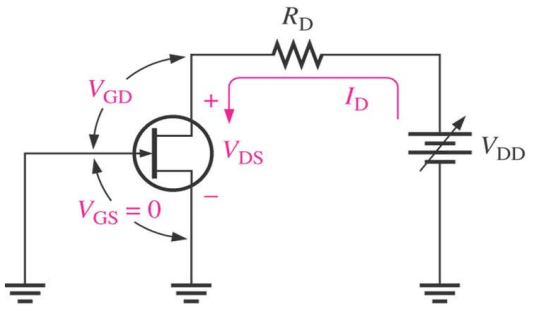


# JFET Characteristics and Parameters Pinch-Off

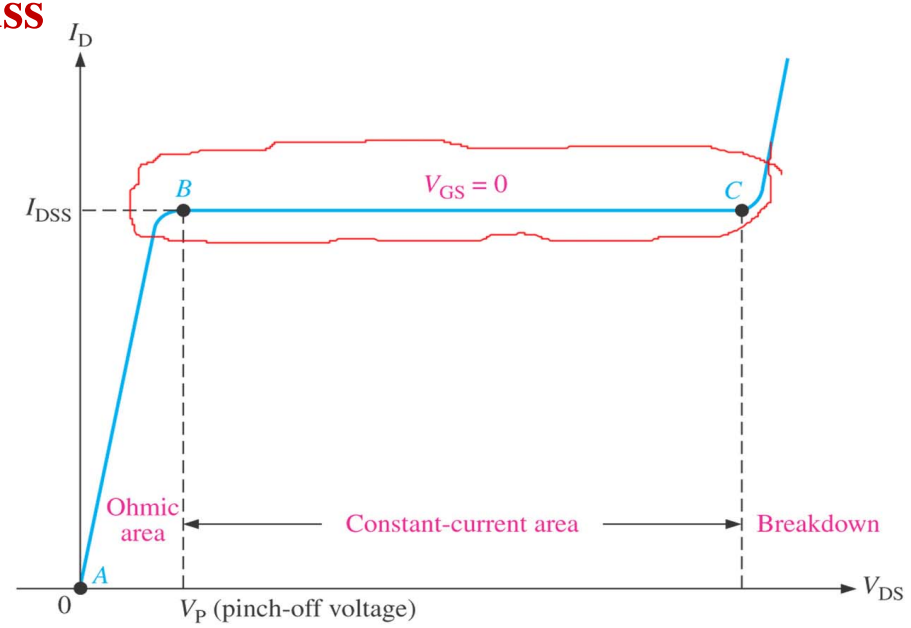
The point when $I_D$ ceases to increase regardless of $V_{DD}$ increases (constant current source) is called the **pinch-off voltage** (point **B**) (*Note*: $V_{GS} = 0$). This current is called maximum drain current ($I_{DSS}$).

**Breakdown** (point C) is reached when too much voltage is applied. This is undesirable, so JFETs operation is always well below this value.

**Pinch off voltage Vp is the value of Vds for Vgs = 0V at which drain current Id becomes constant i.e. Idss**

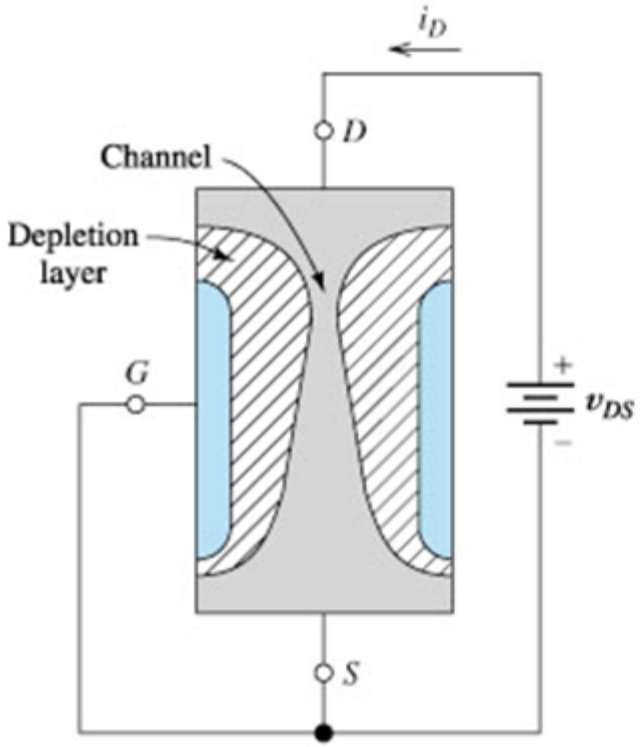



(a) JFET with $V_{GS} = 0$ V and a variable $V_{DS}$ ($V_{DD}$)

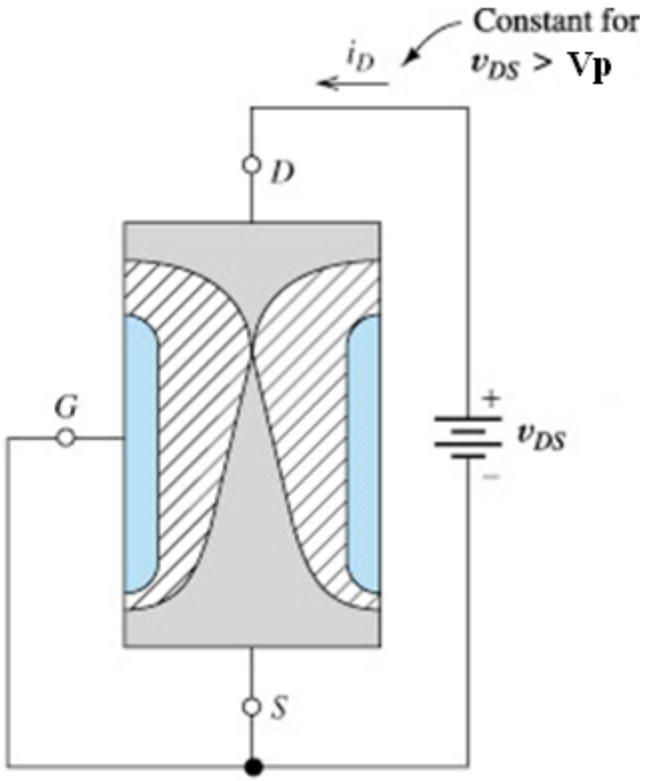



(b) Drain characteristic

# JFET Characteristics and Parameters Pinch-Off




(a) Channel becomes narrower as $v_{DS}$ is increased



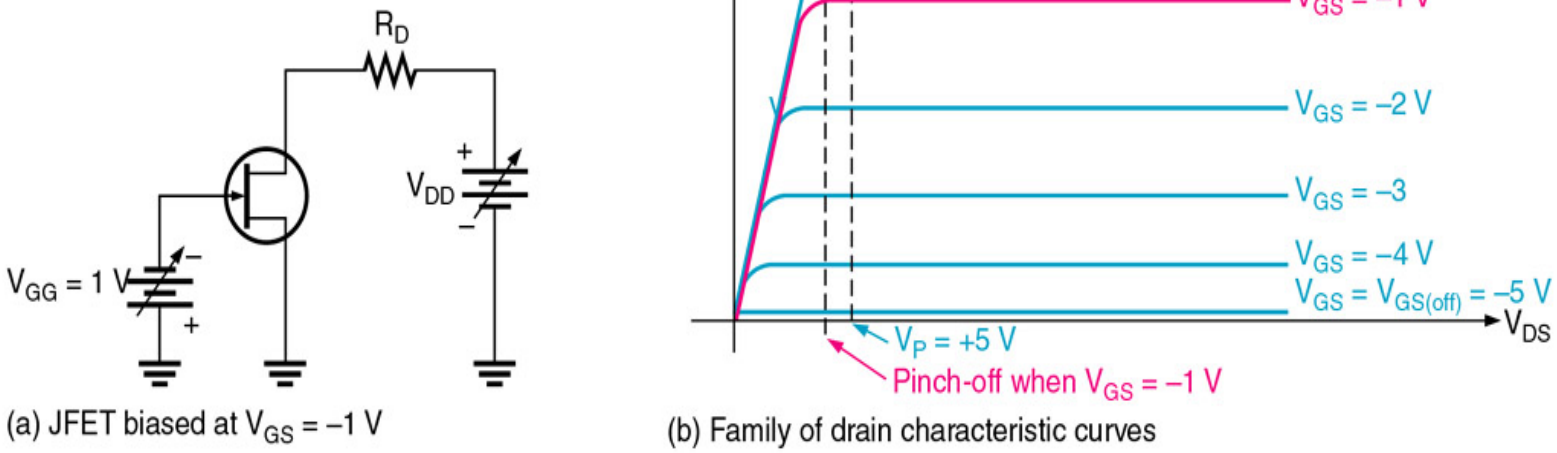

(b) Current is confined to a very narrow strip for $v_{DS}$ > Vp

# JFET Characteristics and Parameters Drain Curves

From this set of curves you can see increased negative voltage applied to the gate (↓-$V_{GS}$) produces no change in $I_D$. $I_D$ is limited and the pinch-off voltage ($V_P$) is reduced.

Note: VGS controls IDSS

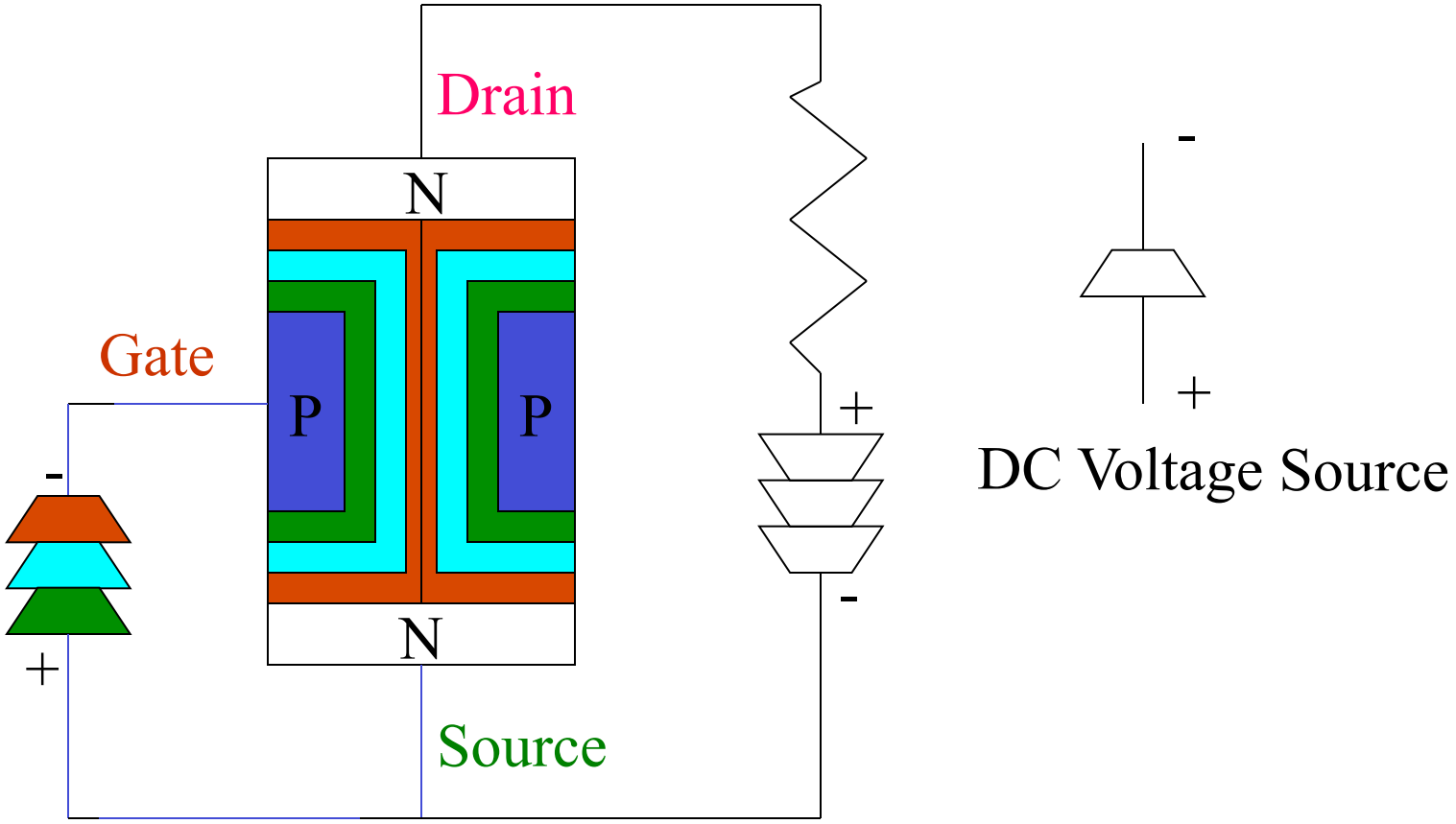
This is the normal work zone for a JFET




(a) JFET biased at $V_{GS}$ = –1 V

(b) Family of drain characteristic curves

# Operation of a JFET



# JFET Characteristics and Parameters Cutoff

We know that as $V_{GS}$ is increased $I_D$ will decrease.

The point that $I_D$ ceases to increase is called cutoff.

The amount of $V_{GS}$ required to do this is called the **cutoff voltage** ($V_P$).

The depletion region grows such that it allows practically no current to flow through.

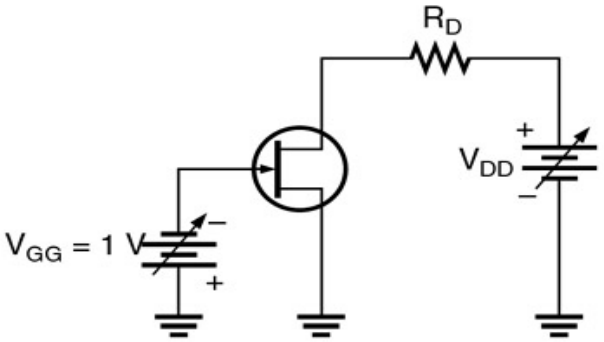
**Cutoff voltage is the value of Vgs called Vgs(off) at which drain current Id ceases to flow.**

It is interesting to note that pinch-off voltage ($V_{GS(off)}$) and cutoff voltage ($V_P$) are the same value but opposite polarity.

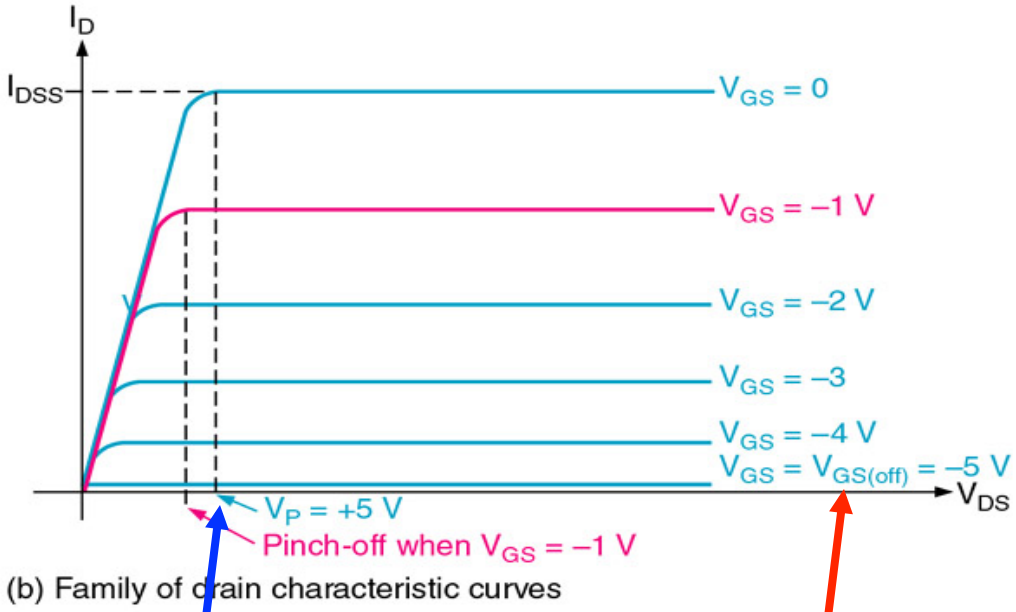
# Pinch-Off "$V_p$" vs Cutoff "$V_{GS(off)}$"

- $V_{GS(off)}$ and $V_P$ are always = and opposite is sign
- $V_{P(inch\ off)}$ - the value of $V_{DS}$ where $I_D$ becomes constant with $V_{GS}$ = 0.
- $V_{P(inch\ off)}$ also occurs for $V_{DS}<V_P$ if $V_{GS} \neq 0$.

  Note: Although $V_P$ is constant, $V_{DSmin}$ where $I_D$ is constant, varies.




(a) JFET biased at $V_{GS} = -1$ V




(b) Family of drain characteristic curves

See Example 7-1

Vp=+5V

VGS(off)= -5V

# JFET Characteristic

- Output characteristic (Drain Characteristic).

  Curve drawn between $I_D$ and Drain Source voltage $V_{DS}$ with gate source voltage $V_{GS}$ as parameter.

- Transfer Characteristic.

  Curve between $I_D$ and $V_{GS}$

# Output or Drain ($V_D$-$I_D$) Characteristics of n-JFET

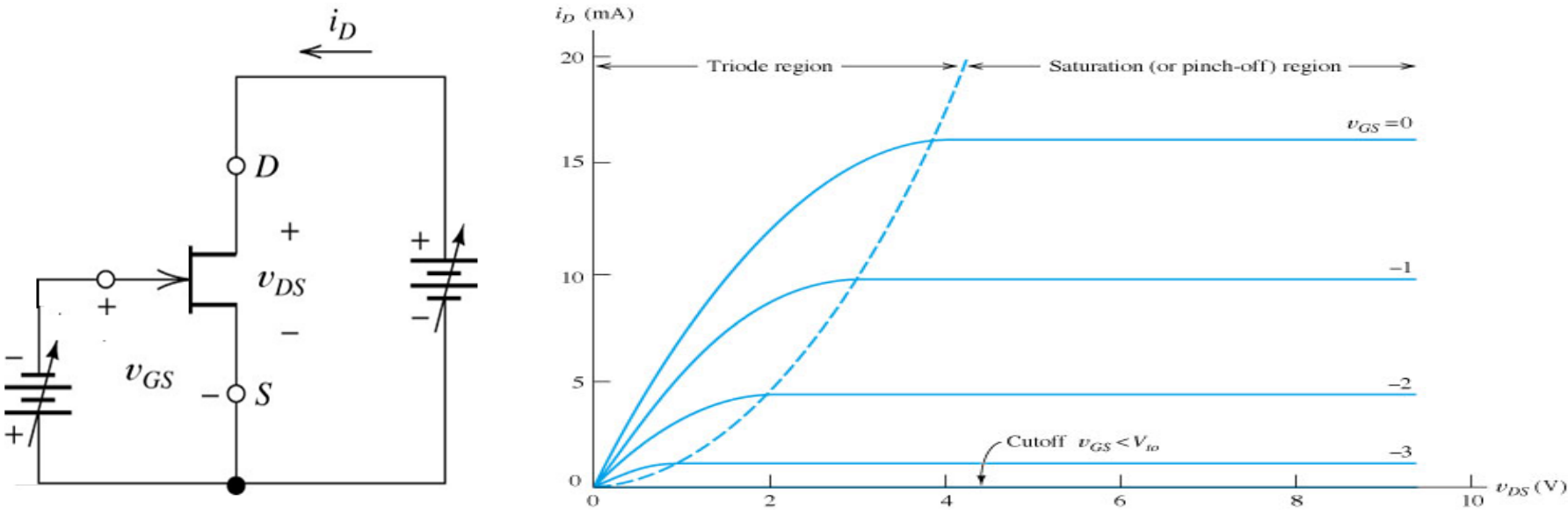



**Figure:** Circuit for drain characteristics of the *n*-channel JFET and its Drain characteristics.

# N-Channel JFET Characteristics and Breakdown

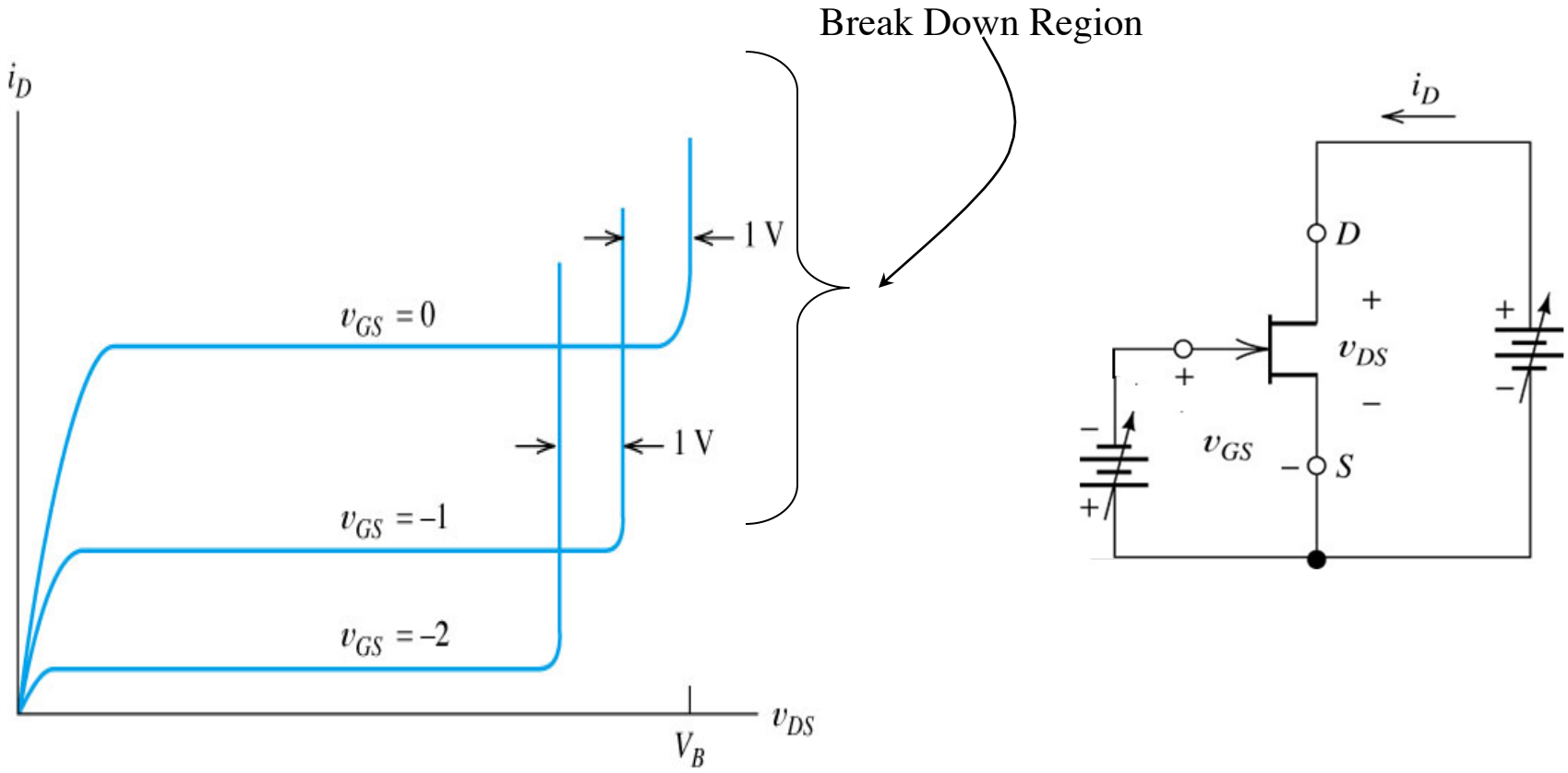



**Figure:** If $v_{DG}$ exceeds the breakdown voltage $V_B$, drain current increases rapidly.

# Regions of a JFET Operation

**Cut-off region:**

The transistor is off.

There is no conduction between the drain and the source when the gate-source voltage is greater than the cut-off voltage.

($I_D = 0$ for $V_{GS} > V_{GS,off}$)

**Active region (also called the Saturation region / Pinch off Region ):**

The transistor is on.

The drain current is controlled by the gate-source voltage ($V_{GS}$) and relatively insensitive to $V_{DS}$.

In this region the transistor can be an amplifier.

In the active region:

$$V_{DS} \geq \left(V_{GS} - V_P\right)$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS,off}}\right)^2$$

Where, $I_{DSS}$ is the short circuit drain current, $V_P$ is the pinch off voltage

## Ohmic region (Non Saturation Region) :

The transistor is on, but behaves as a voltage controlled resistor. When $V_{DS}$ is less than in the active region, the drain current is roughly proportional to
the source-drain voltage and is controlled by the gate voltage. In the ohmic region drain current is given by:

$$V_{DS} < \left( V_{GS} - V_P \right)$$

$$I_{DS} = \frac{2I_{DSS}}{V_P^2} \left[ \left( V_{GS} - V_P \right) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

Where, $I_{DSS}$ is the short circuit drain current, $V_P$ is the pinch off voltage

# Transfer Characteristics of n-Channel JFET

The *transfer characteristic curve* illustrates the control $V_{GS}$ has on $I_D$ from cutoff ($V_{GS(off)}$ ) to pinch-off ($V_P$). Note the parabolic shape. The formula below can be used to determine drain current.

$$I_D = I_{DSS}\,(1 - V_{GS}/V_{GS(off)})^2$$

Note:($\mathbf{V_{GS} = 0}$ **to** $\mathbf{V_{GS(off)}}$ **controls** $\mathbf{I_D}$)

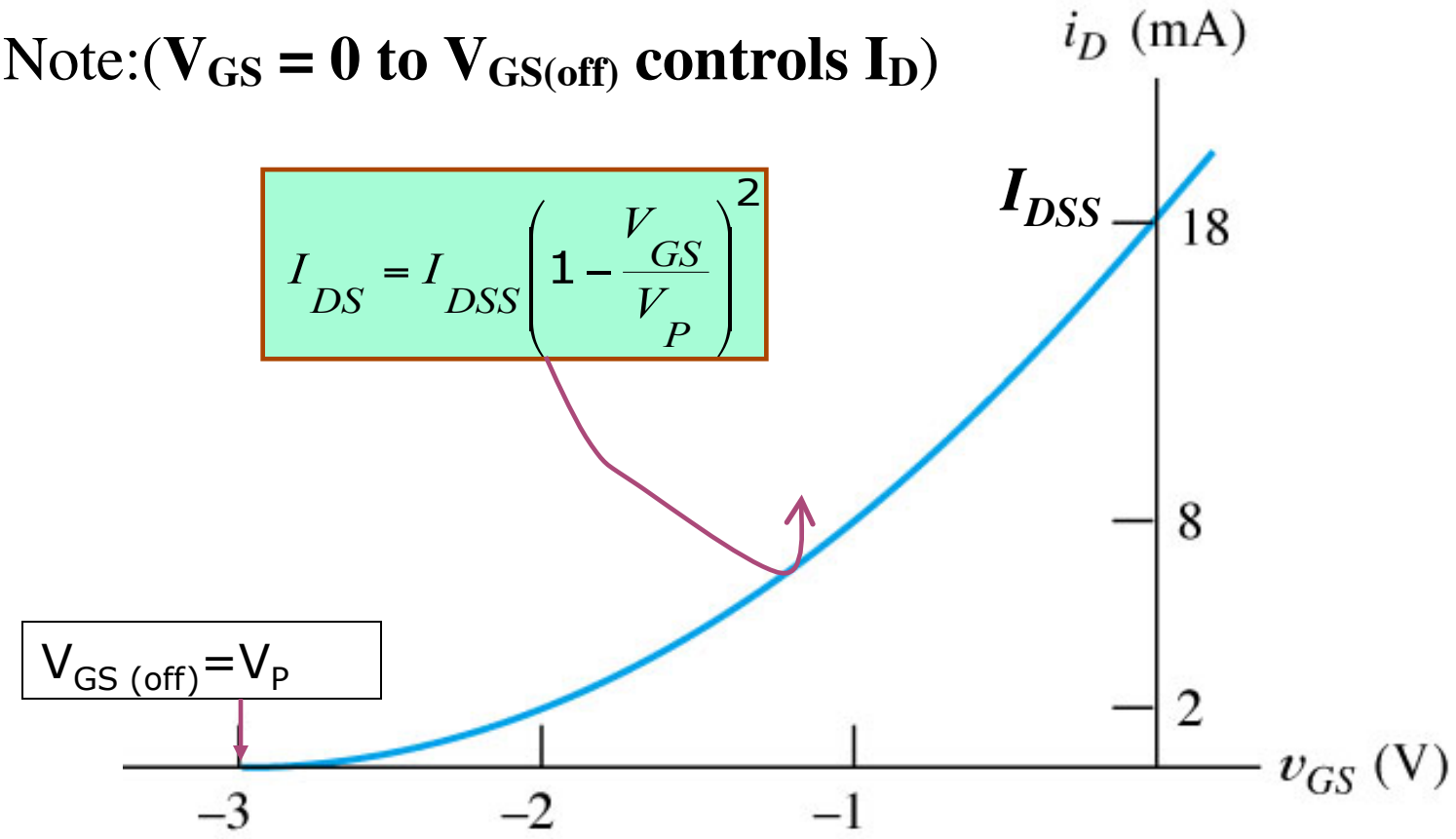
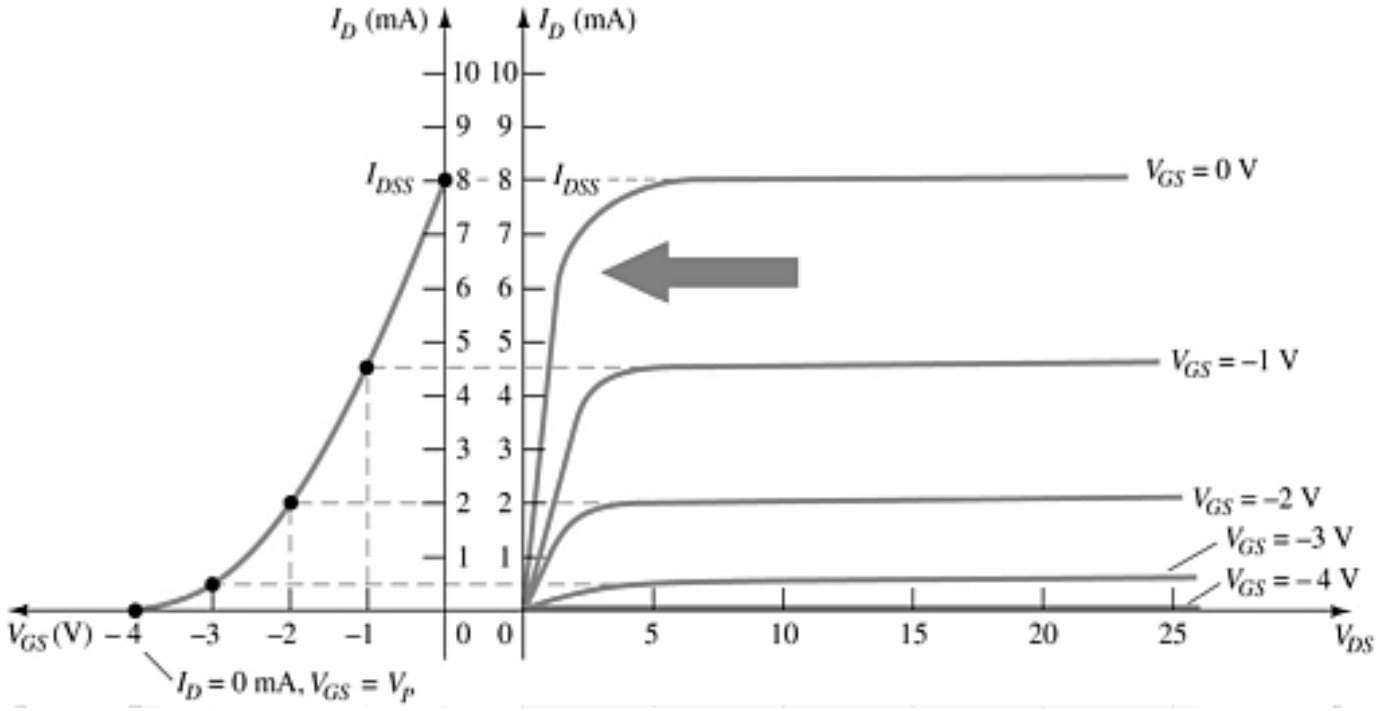



**Figure: Transfer Characteristics of n-Channel JFET**

# JFET Transfer Curve

This graph shows the value of $I_D$ for a given value of $V_{GS}$



# JFET Characteristics and Parameters

## $I_{DSS}$ : Drain Source Saturation Current

Signifies the drain saturation current when $V_{GS} = 0V$.

**Dynamic Drain Resistance** **at an operating point** is the ratio of changes of $V_{DS}$ to $I_D$ keeping the gate source voltage constant. Large changes in $V_{DS}$ produce very small changes in $I_D$.

$$r_d = \Delta V_{DS} / \Delta I_D \text{ (for constant Vgs)}$$

Drain resistance is the AC resistance between the drain and the source terminals when the JFET is operating in the pinch off region.

It is the output resistance of the diode.

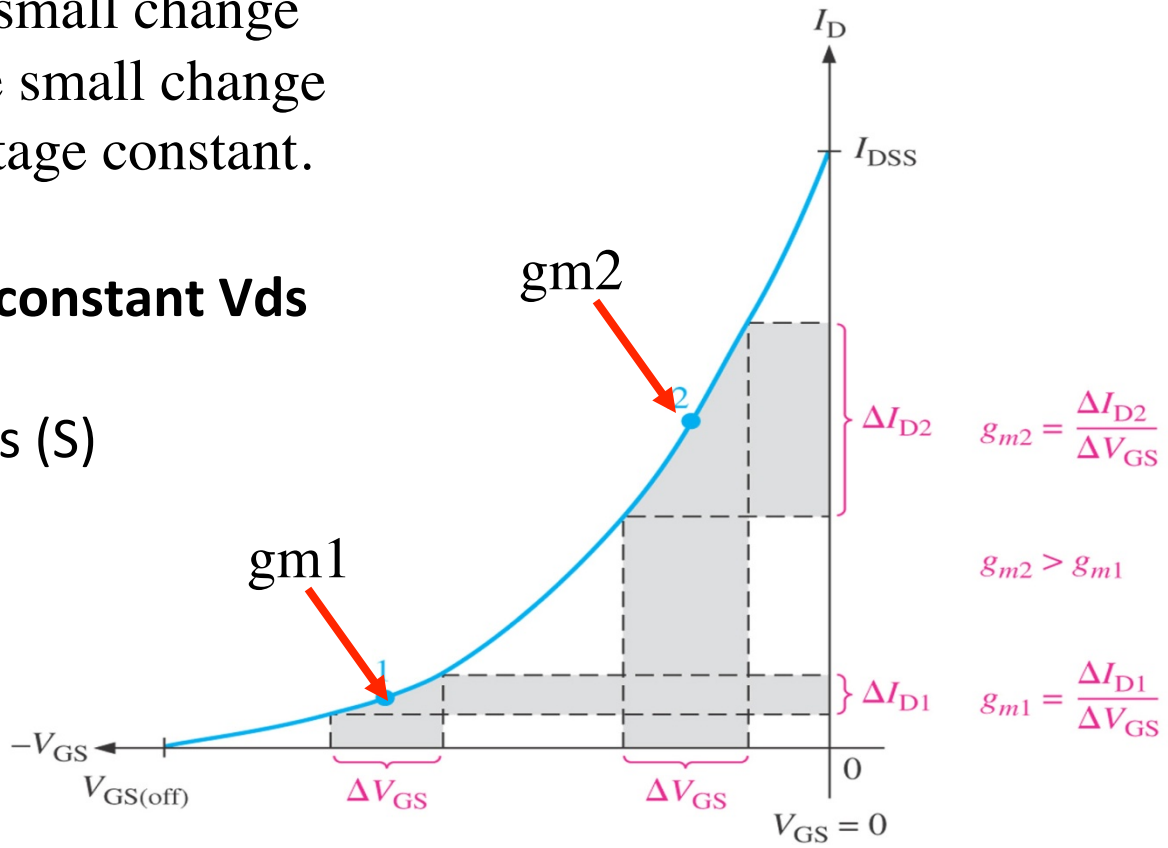
# JFET Characteristics and Parameters

**Forward transfer conductance** (*gm*) (*Forward Transconductance*).

Transconductance at an operating point is defined as the ratio of small change in drain current $I_D$ to the small change in $V_{GS}$ keeping drain voltage constant.

$gm = \Delta I_D / \Delta V_{GS}$ **for constant Vds**

It is measured in Siemens (S)



# JFET Characteristics and Parameters

**Input resistance** for a JFET is high since the gate-source junction is reverse-biased.

$$R_{IN} = |V_{GS}/I_{GSS}|$$

where: $I_{GSS}$ is the "gate reverse current"
@ a certain "gate-to-source" voltage.

Gate Cutoff Current or Gate Reverse Current (IGSS):
The gate channel junction in a JFET is reverse biased, a minority charge carrier current flows called as Gate Source cutoff current or Gate reverse current.

# JFET Characteristics and Parameters

**Amplification Factor** is defined as the ratio of small change in drain voltage $V_{DS}$ to the small change in gate voltage $V_{GS}$ when drain current $I_D$ is kept constant.

$$\mu = \Delta V_{Ds}/\Delta V_{GS} \quad \text{for constant } I_D$$

$$\mu = r_d g_m$$

# JFET Characteristics and Parameters

Breakdown Voltage :

$BV_{DGO}$ : Drain gate breakdown voltage with the source terminal open circuited.

$BV_{GSS}$ : Gate source breakown voltage with drain terminal shorted to the source.

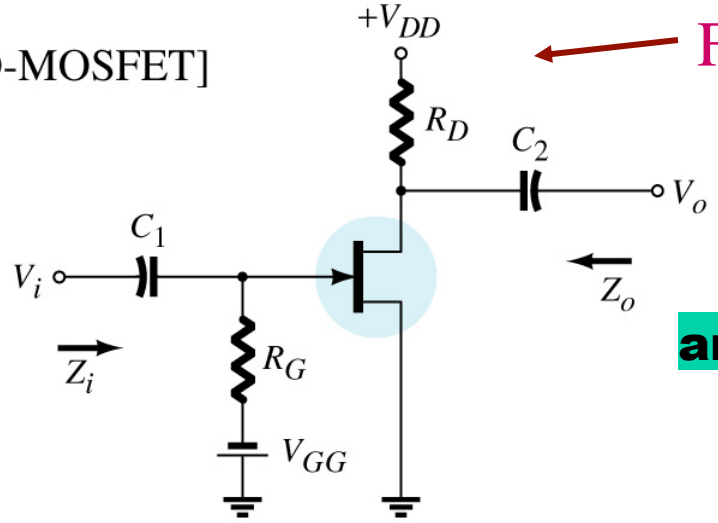
Both are specifications of the voltage at which the gate channel junctions might breakdown.

# Biasing Circuits used for JFET

- Fixed bias circuit
- Self bias circuit
- Potential Divider bias circuit

# JFET (n-channel) Biasing Circuits

Fixed-bias
[JFET or D-MOSFET]




For Fixed Bias Circuit

Applying KVL to gate circuit we get

$$V_{GG} = I_G R_G + V_{GS} = V_{GS} = Fixed, \because I_G = 0$$

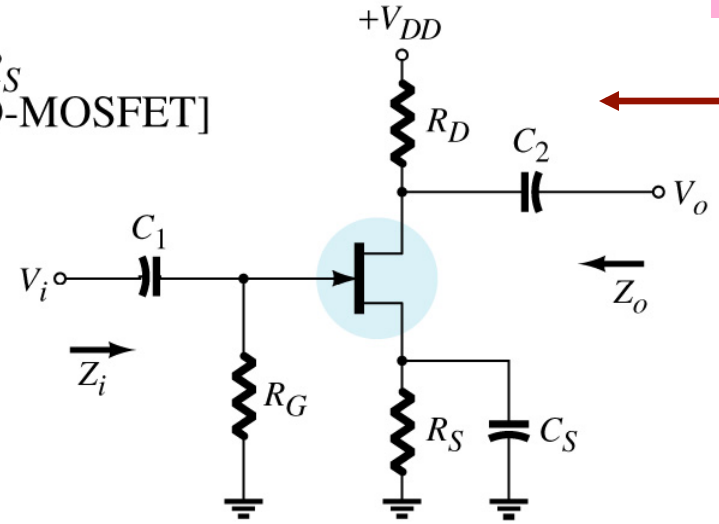
and

$$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$\text{and } V_{DS} = V_{DD} - I_{DS} R_D$$

Where, $V_p = V_{GS\text{-}off}$ & $I_{DSS}$ is Short ckt. $I_{DS}$

Self-bias
bypassed $R_S$
[JFET or D-MOSFET]



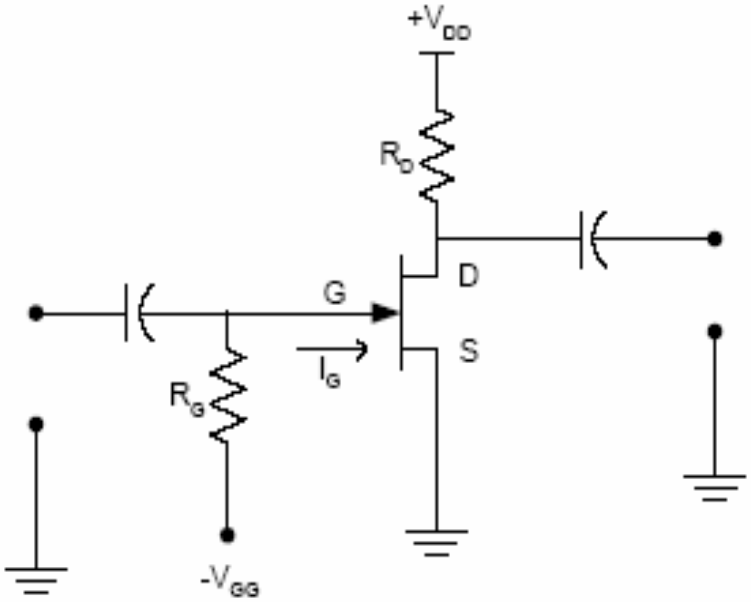

For Self Bias Circuit

$$V_{GS} + I_{DS} R_S = 0$$

$$\therefore I_{DS} = -\frac{V_{GS}}{R_S}$$

# JFET Biasing Circuits Count…

Gate Bias: or Fixed Bias Ckt.




Since $I_G = 0$,

$$V_{GS} = V_{GG}$$

$$V_{DS} = V_{DD} - I_D R_D$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

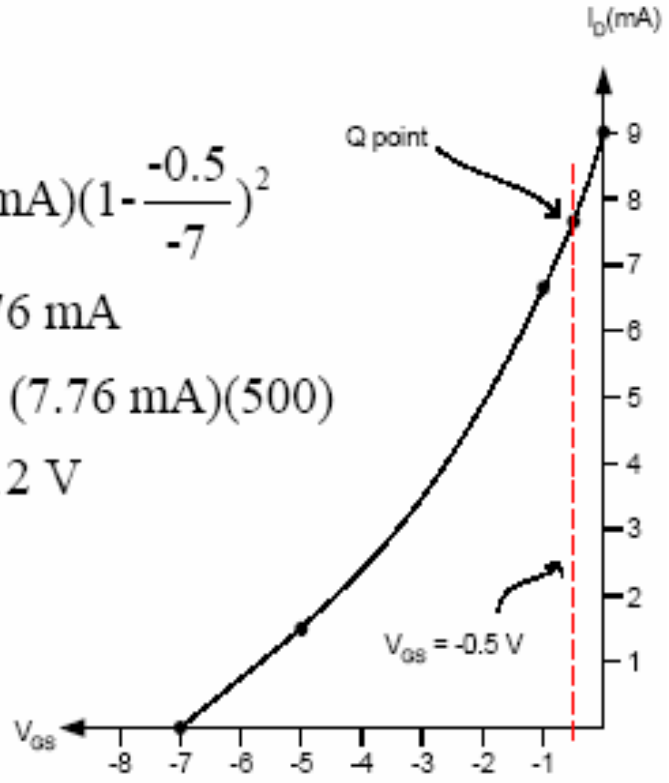
- Example: Determine the Q-point values for the gate biasing circuit if $V_{GG} = -0.5$ V, $V_{GS(off)} = -7$ V, $I_{DSS} = 9$ mA, $V_{DD} = 5$ V and $R_D = 500\Omega$.

$$I_D = (9\text{mA})\left(1 - \frac{-0.5}{-7}\right)^2$$

$$= 7.76 \text{ mA}$$

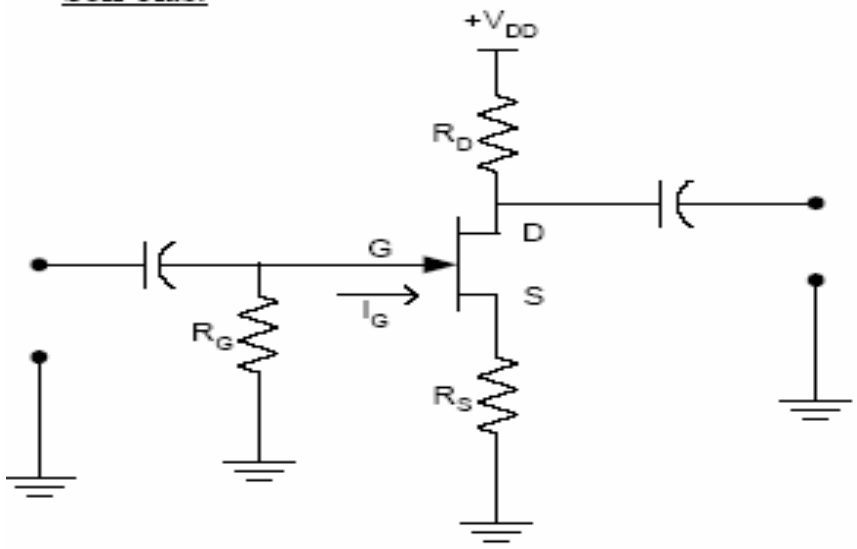
$$V_{DS} = 5 - (7.76 \text{ mA})(500)$$

$$= 1.12 \text{ V}$$



# JFET Self (or Source) Bias Circuit

Self bias:




Since $I_G = 0$ , $V_G = 0$

$V_S = I_D R_S$

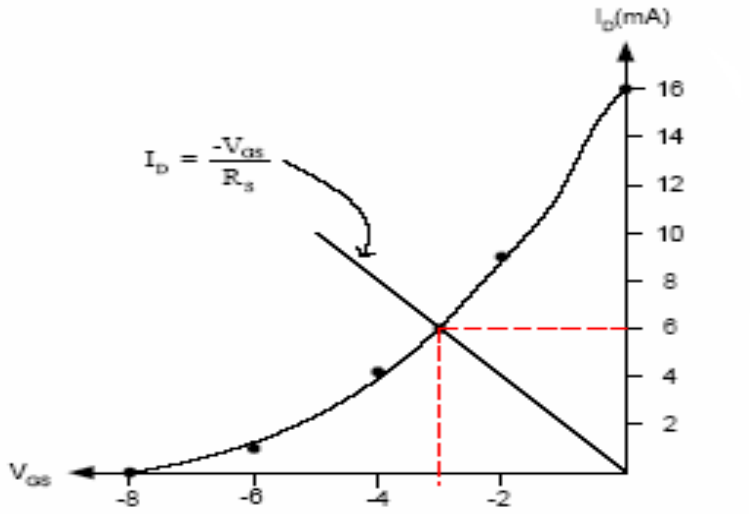
$V_{GS} = -I_D R_S$

$I_D = \dfrac{-V_{GS}}{R_S}$

$V_{DS} = V_{DD} - I_D(R_D + R_S)$

and $I_{DS} = I_{DSS}\left(1 - \dfrac{V_{GS}}{V_P}\right)^2$

- Example: Determine the Q-point values for the self biasing circuit if $V_{GS(off)} = -8$ V , $I_{DSS} = 16$ mA , $V_{DD} = 10$ V , $R_D = 500\ \Omega$ , $R_G = 1$ M$\Omega$ and $R_S = 500\ \Omega$.




$I_D = 6$ mA

$V_{DS} = 10 - (6\text{mA})(500+500)$

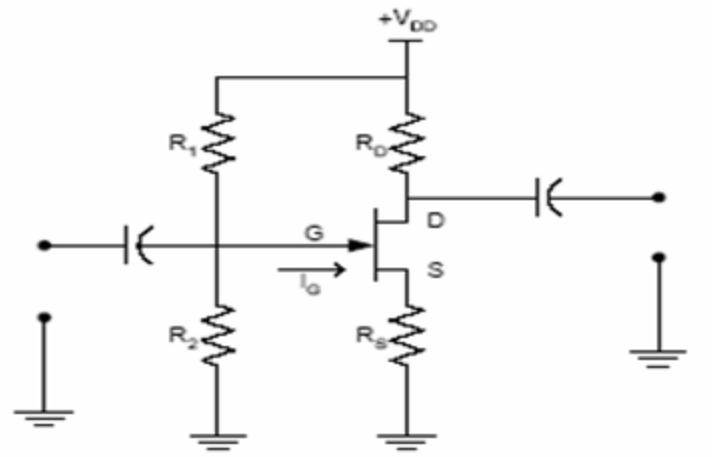
$= 4$ V

$$I_{DSS}\left[1 - 2\frac{V_{GS}}{V_P} + \left(\frac{V_{GS}}{V_P}\right)^2\right] + \frac{V_{GS}}{R_S} = 0$$

This quadratic equation can be solved for $V_{GS}$ & $I_{DS}$

# The Potential (Voltage) Divider Bias

Voltage-divider bias:




Since $I_G = 0$ ,

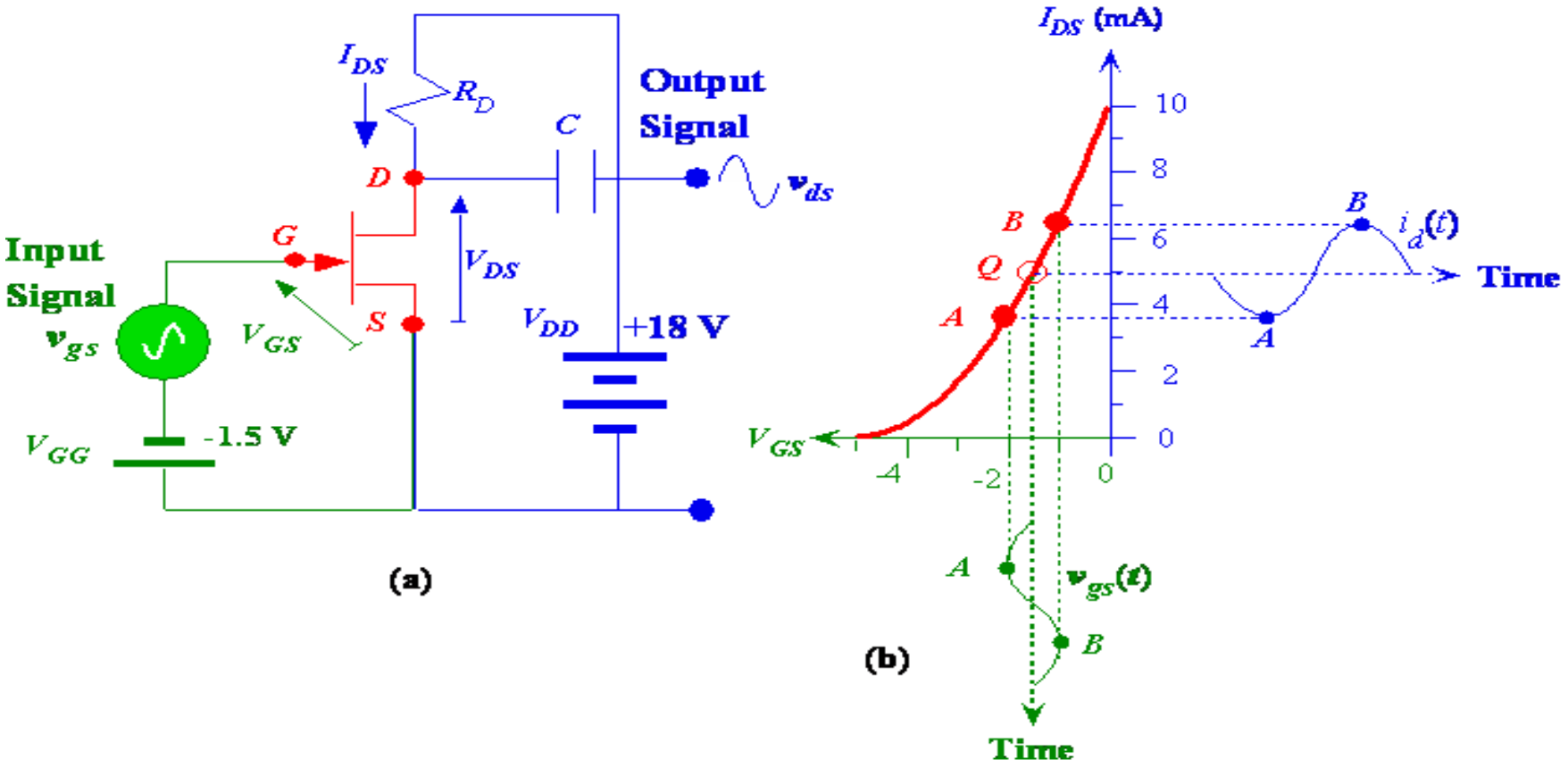
$$V_G = \frac{R_2}{R_1 + R_2} V_{DD}$$

$$I_D = \frac{V_S}{R_S} = \frac{V_G - V_{GS}}{R_S}$$

$$\therefore I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 - \frac{V_G - V_{GS}}{R_S} = 0$$

Solving this quadratic equation gives $V_{GS}$ *and* $I_{DS}$

# A Simple CS Amplifier and Variation in $I_{DS}$ with $V_{gs}$




(a) Common source (CS) ac amplifier using a JFET.
(b) Explanation of how $I_D$ is modulated by the signal $v_{gs}$ in series with the dc bias voltage $V_{GG}$

# MOSFET

## METAL OXIDE SEMICONDUCTOR FET

## IGFET (INSULATED GATE FET)

- Importance for LSI/VLSI
  - Low fabrication cost
  - Small size
  - Low power consumption
- Applications
  - Microprocessors
  - Memories
  - Power Devices
- Basic Properties
  - Unipolar device
  - Very high input impedance
  - Capable of power gain
  - 3/4 terminal device, G, S, D, B
  - Two possible device types: enhancement mode; depletion mode
  - Two possible channel types: n-channel; p-channel

# ENHANCEMENT MOSFET

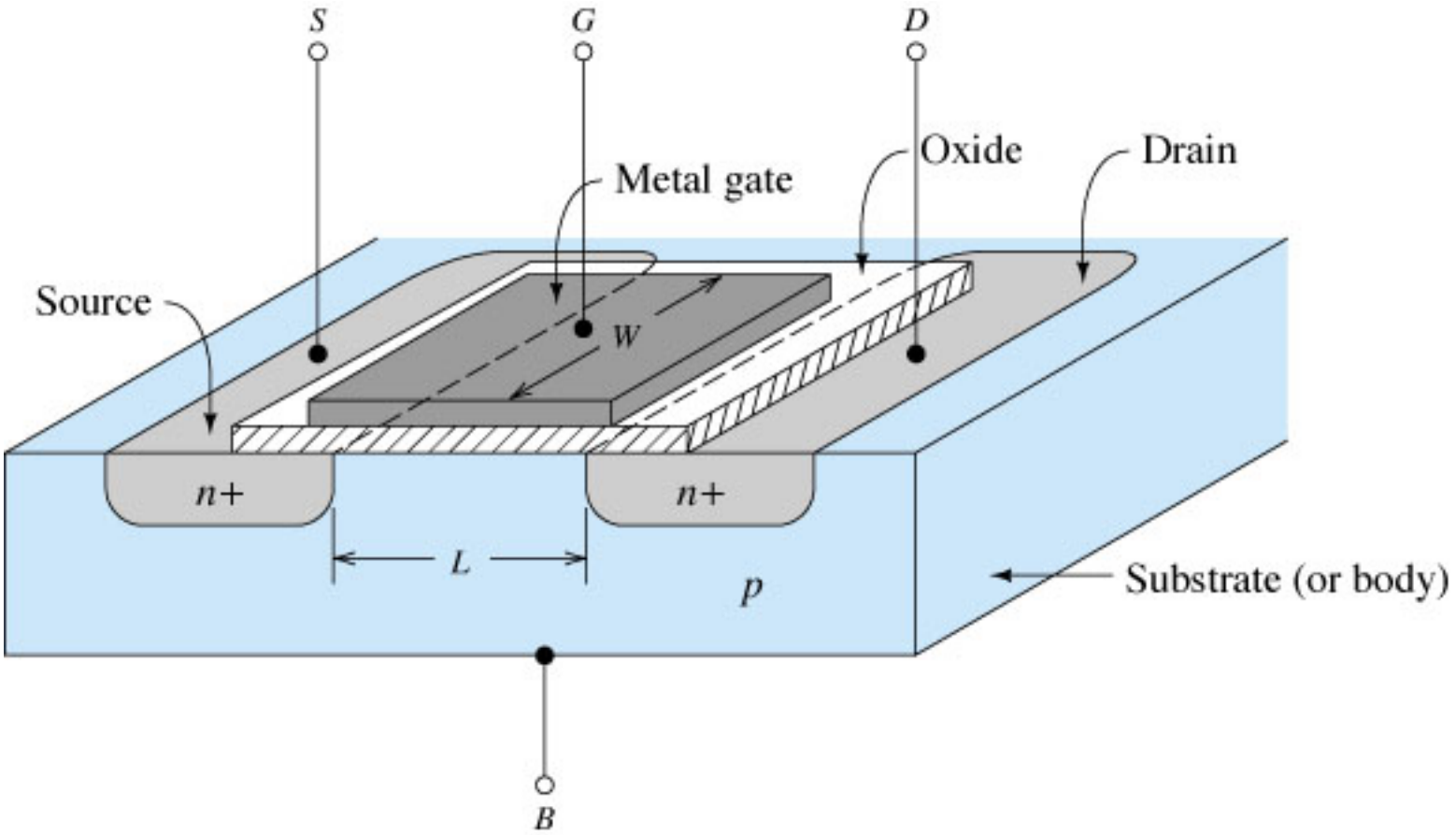



**Figure:** *n*-Channel Enhancement MOSFET showing channel length *L* and channel width *W*.

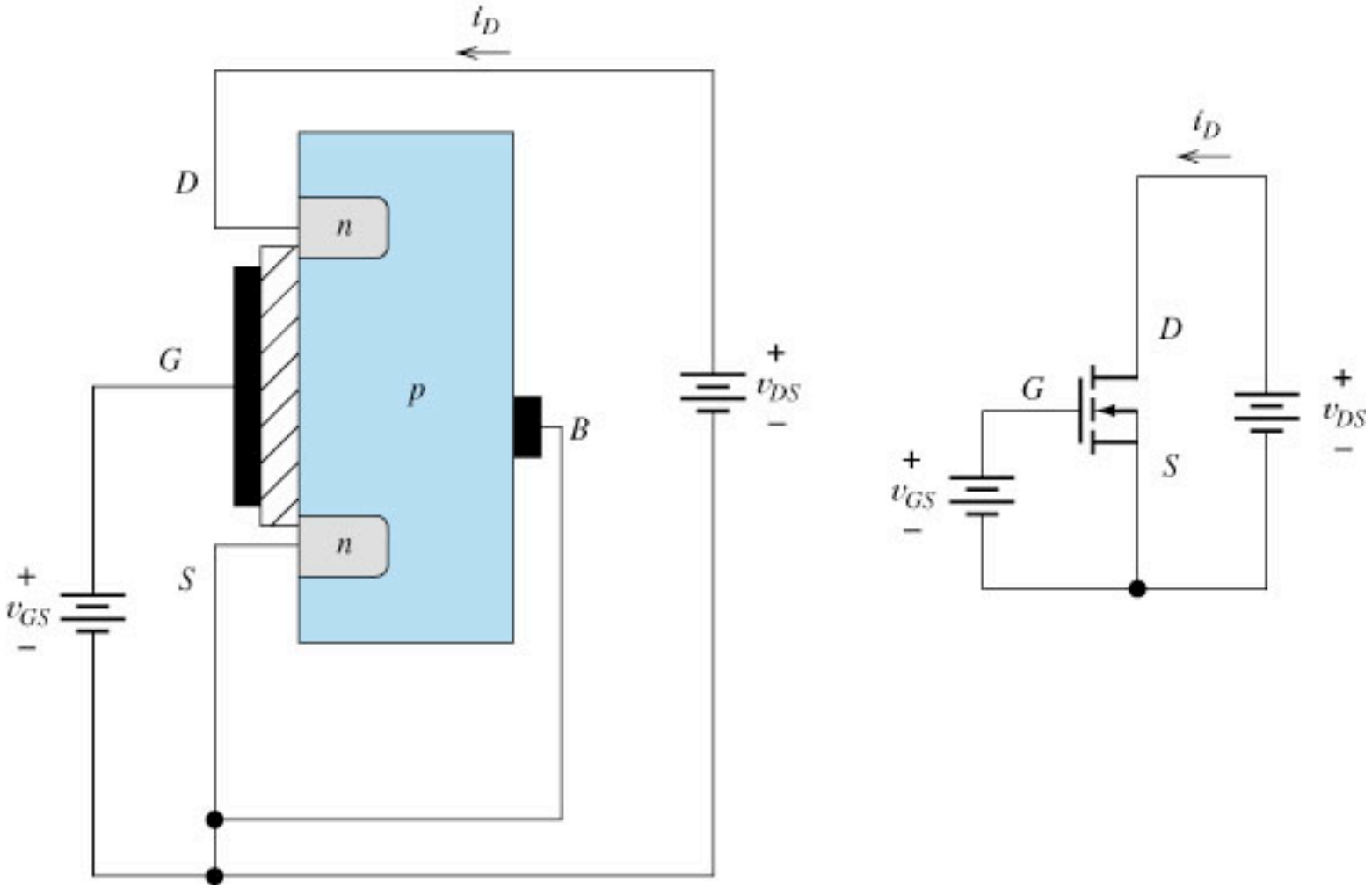



**Figure:** For $v_{GS} < V_{to}$ the *pn* junction between drain and body is reverse biased and $i_D$=0.

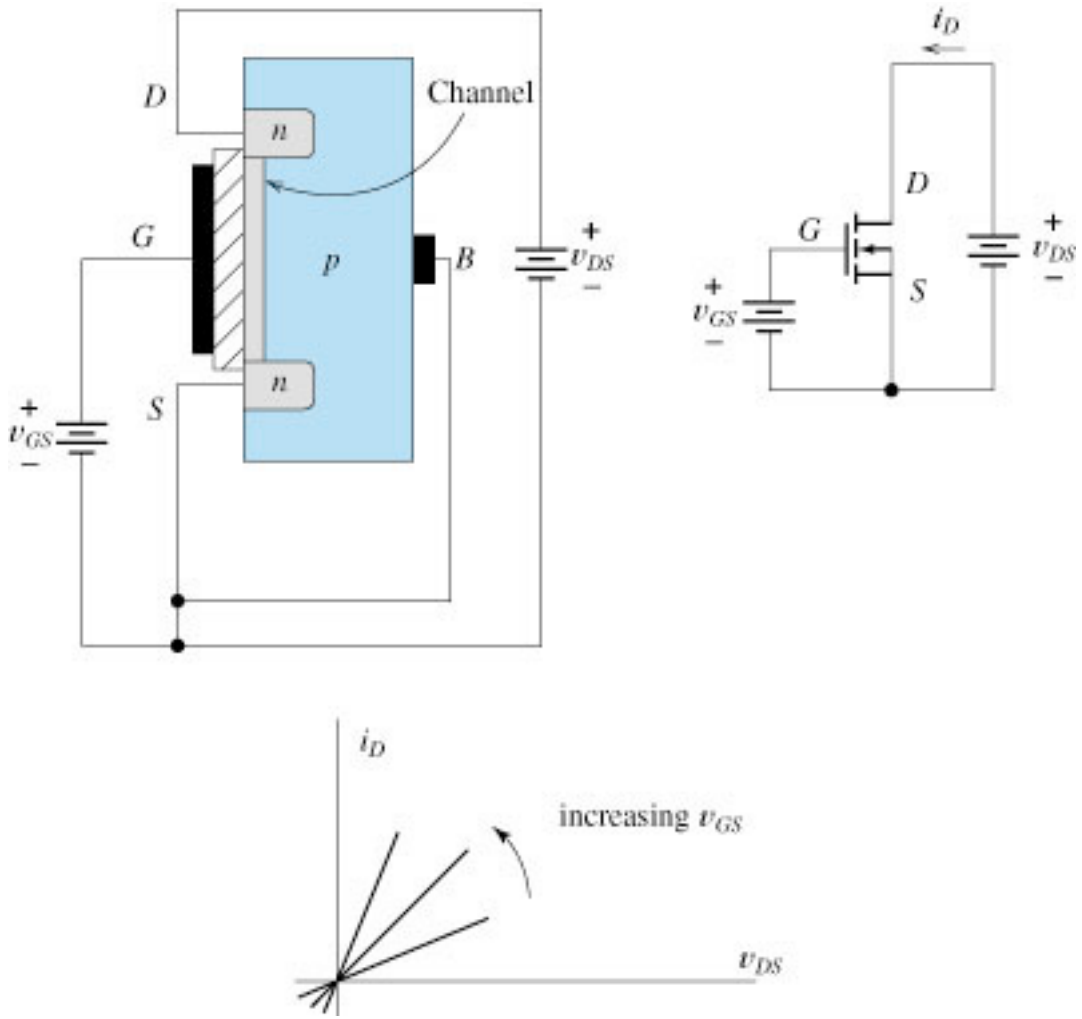



**Figure:** For $v_{GS} > V_{to}$ a channel of *n*-type material is induced in the region under the gate. As $v_{GS}$ increases, the channel becomes thicker. For small values of $v_{DS}$ ,$i_D$ is proportional to $v_{DS}$. The device behaves as a resistor whose value depends on $v_{GS}$.

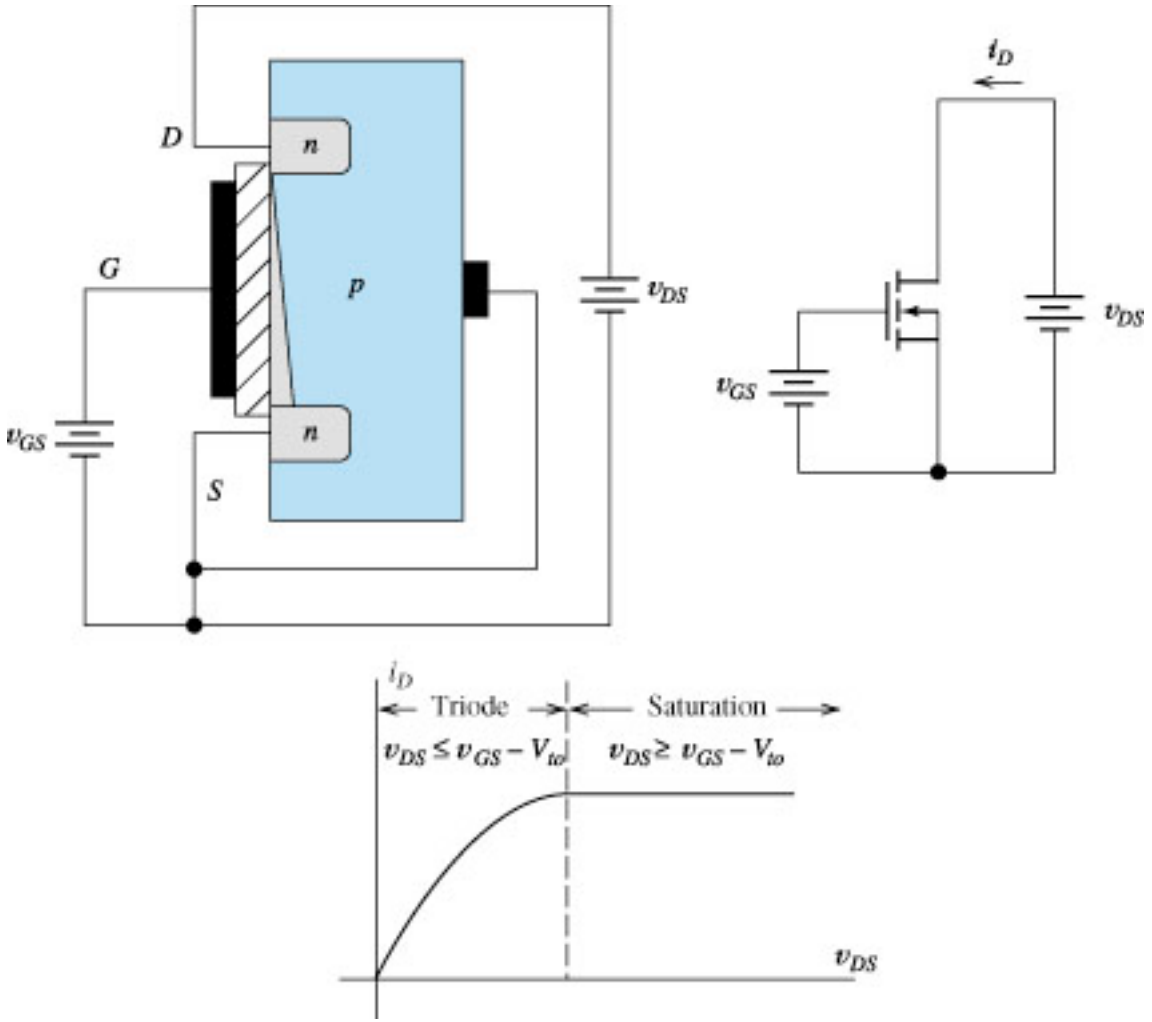
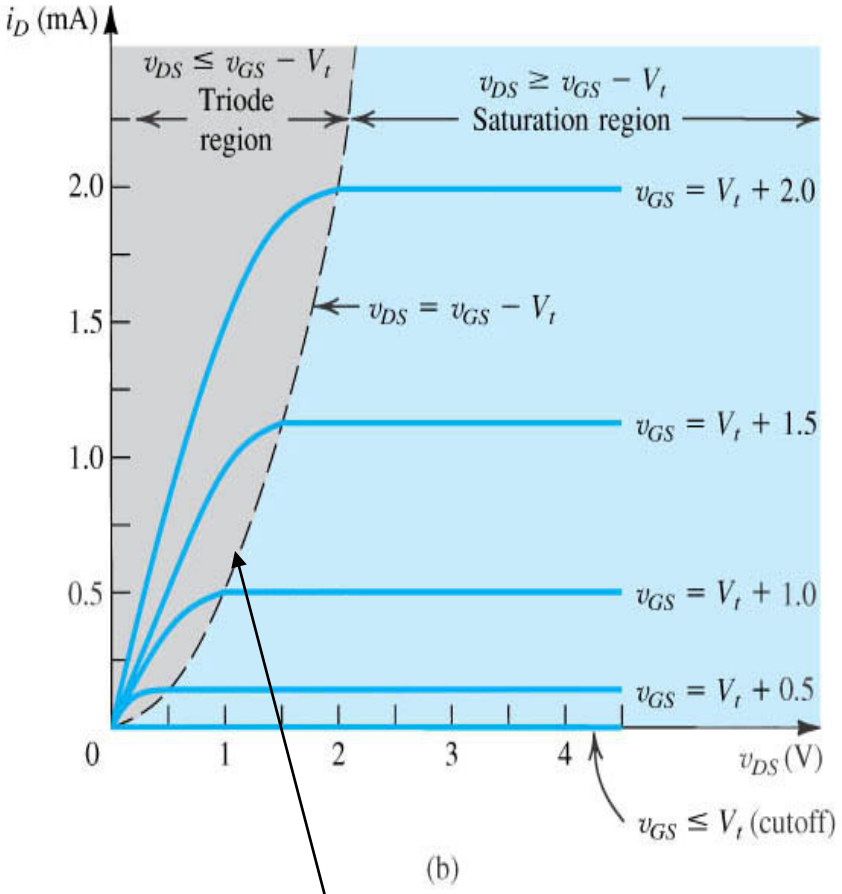
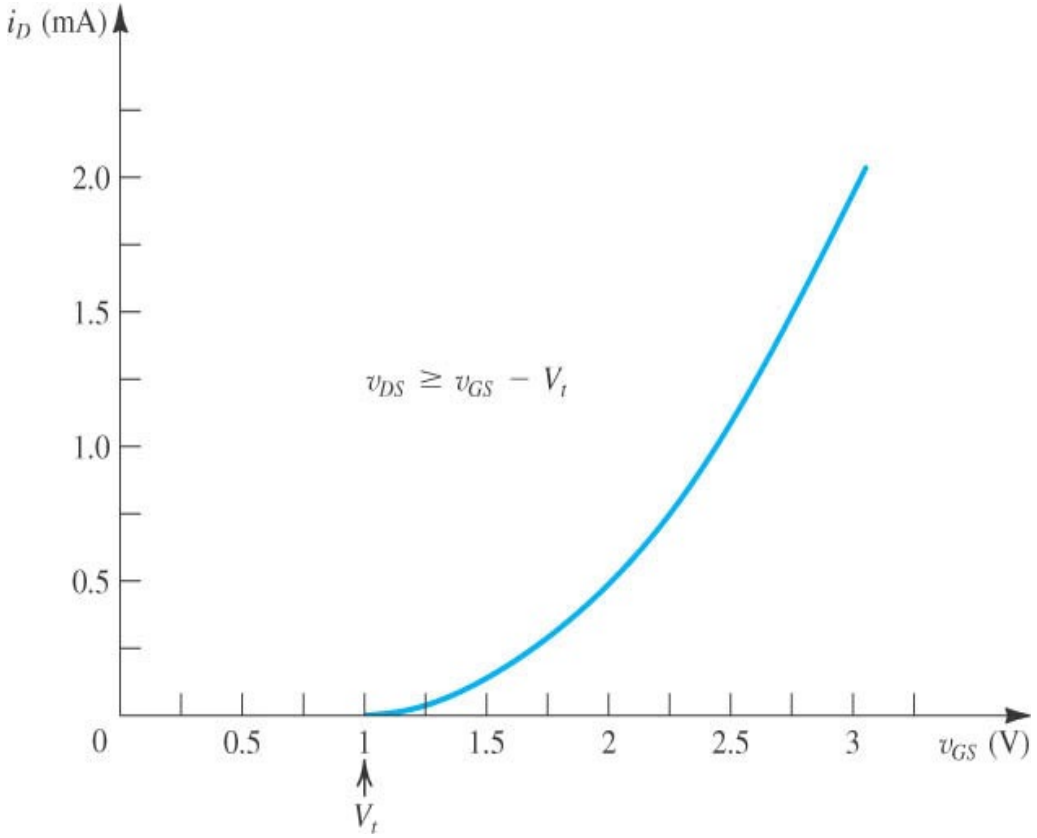



**Figure:** As $v_{DS}$ increases, the channel pinches down at the drain end and $i_D$ increases more slowly. Finally for $v_{DS} > v_{GS} - V_{to}$, $i_D$ becomes constant.

# Current-Voltage Relationship of n-EMOSFET




Locus of points where

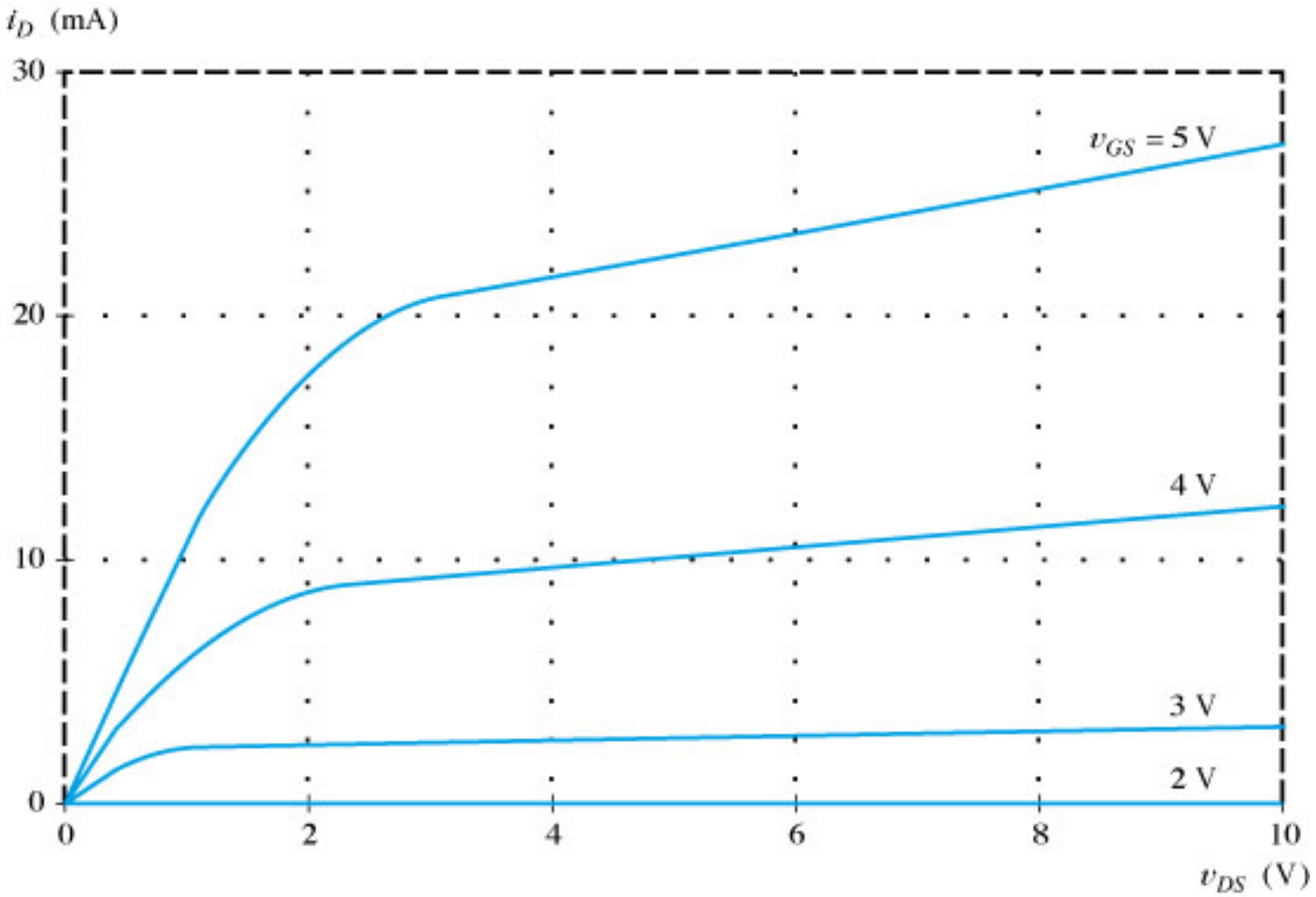



**Figure:** Drain characteristics

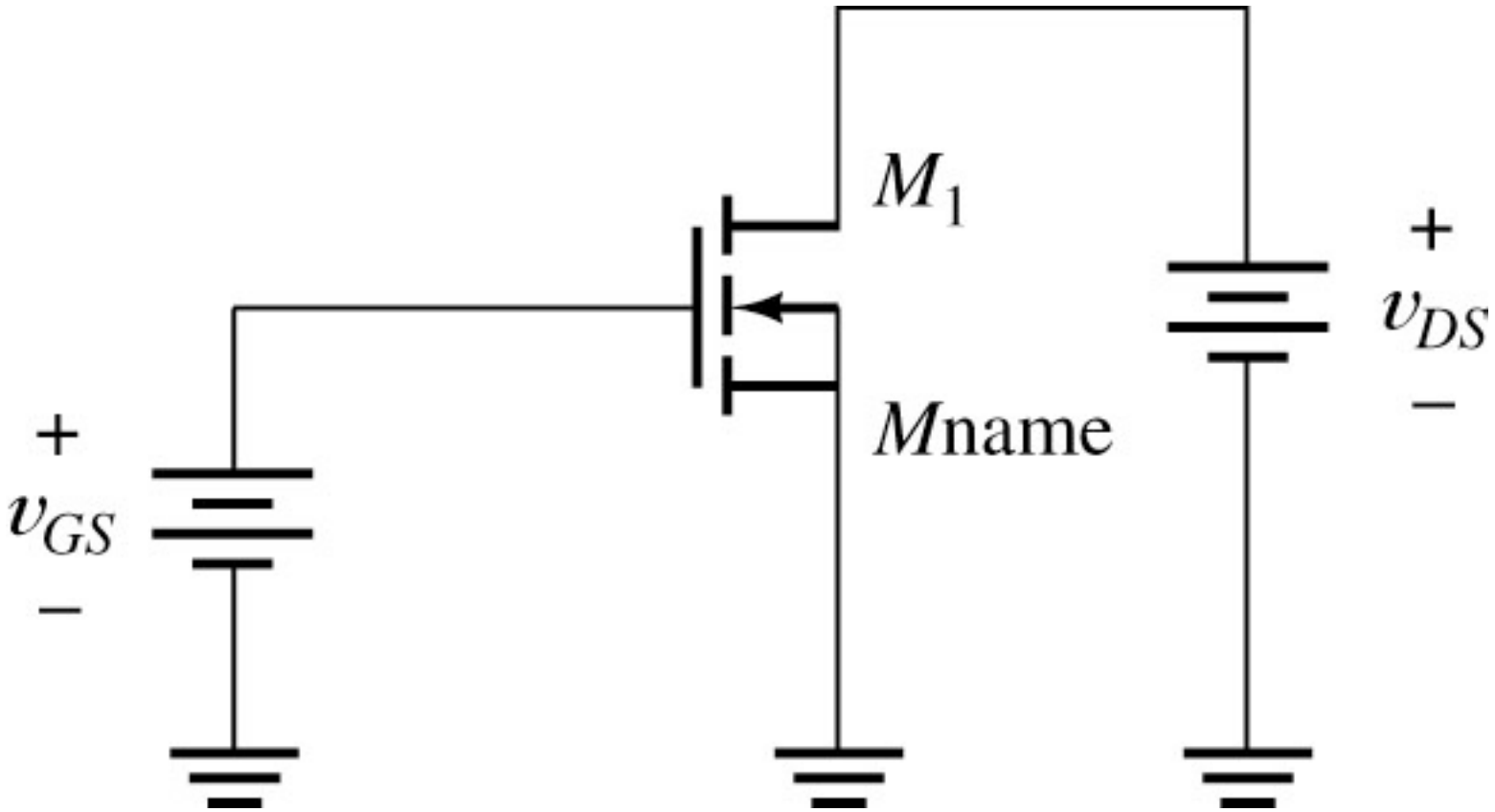



**Figure:** This circuit can be used to plot drain characteristics.

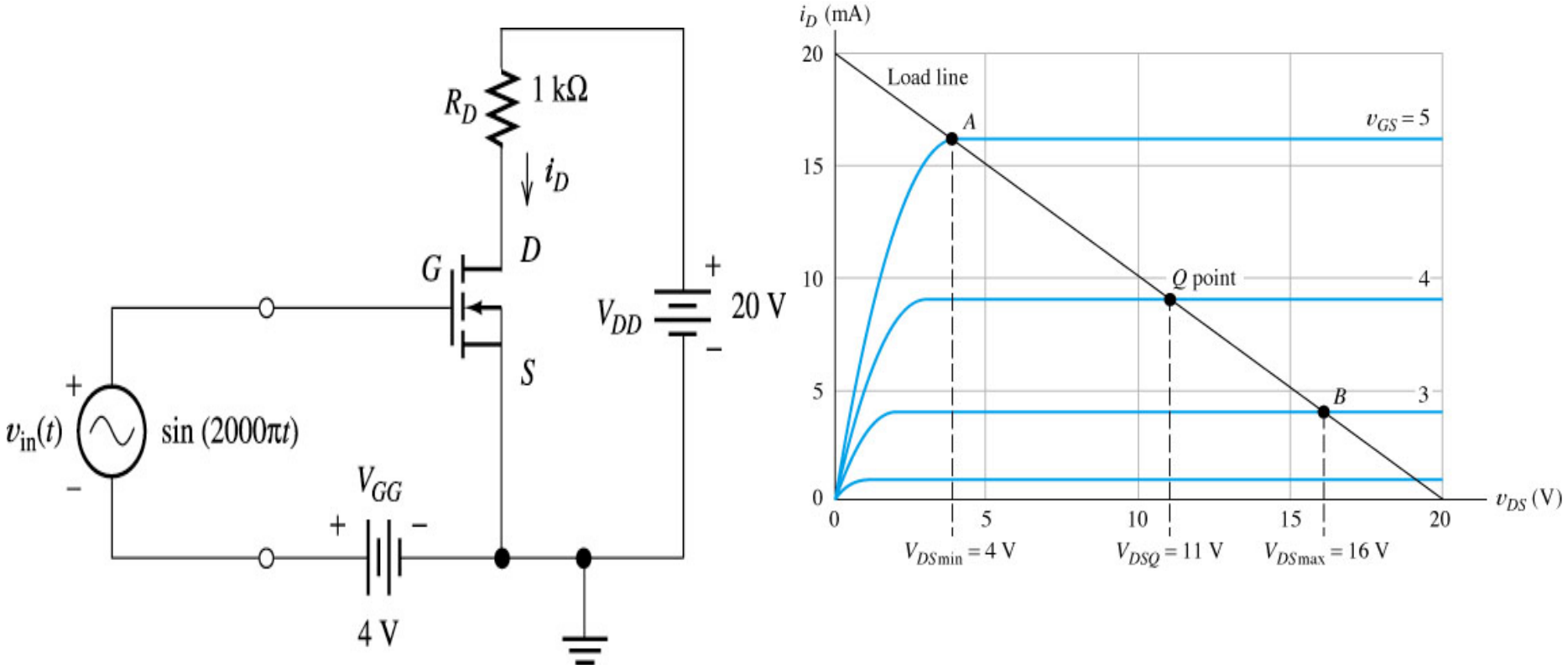



**Figure:** Simple NMOS amplifier circuit and Characteristics with load line.

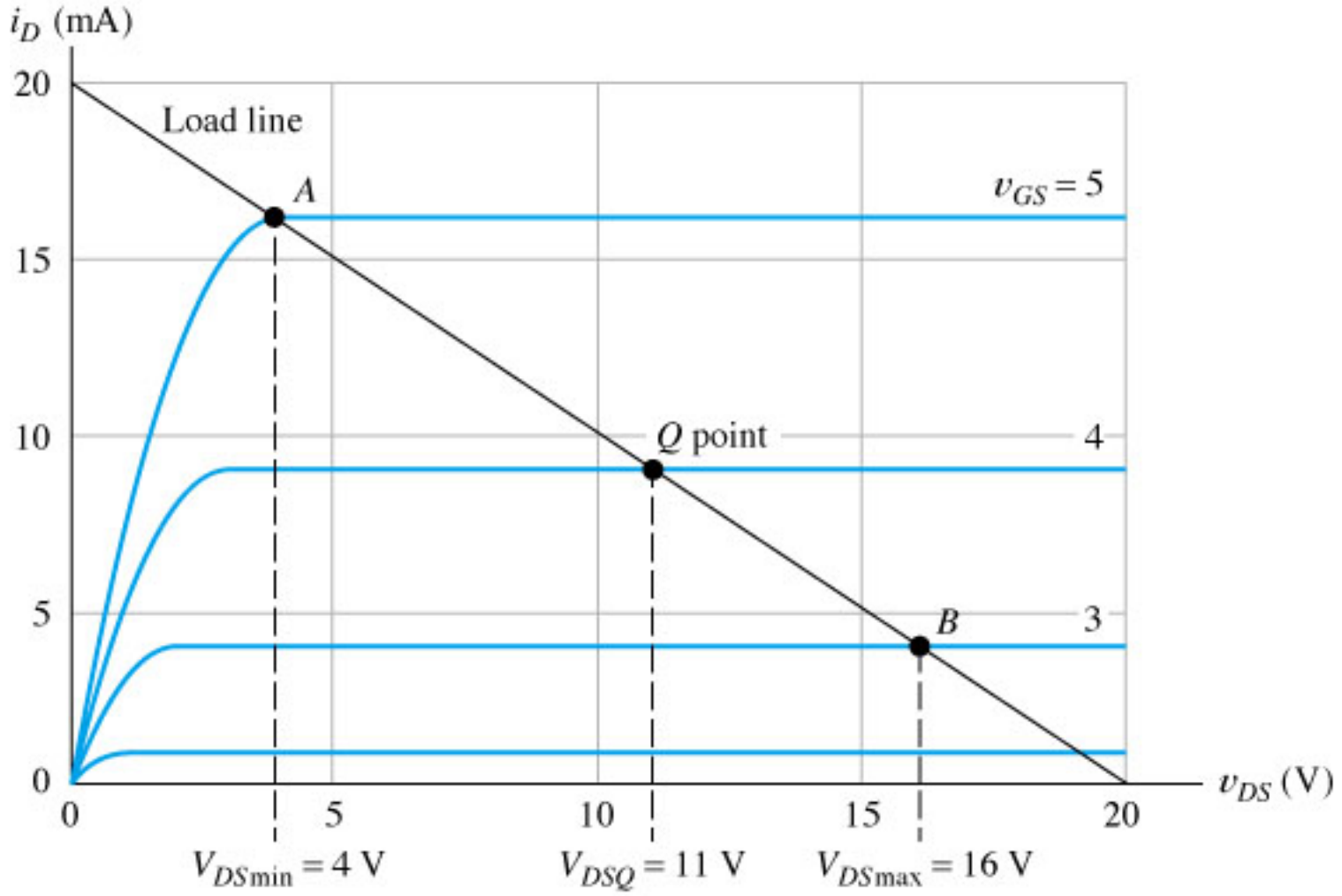



**Figure:** Drain characteristics and load line

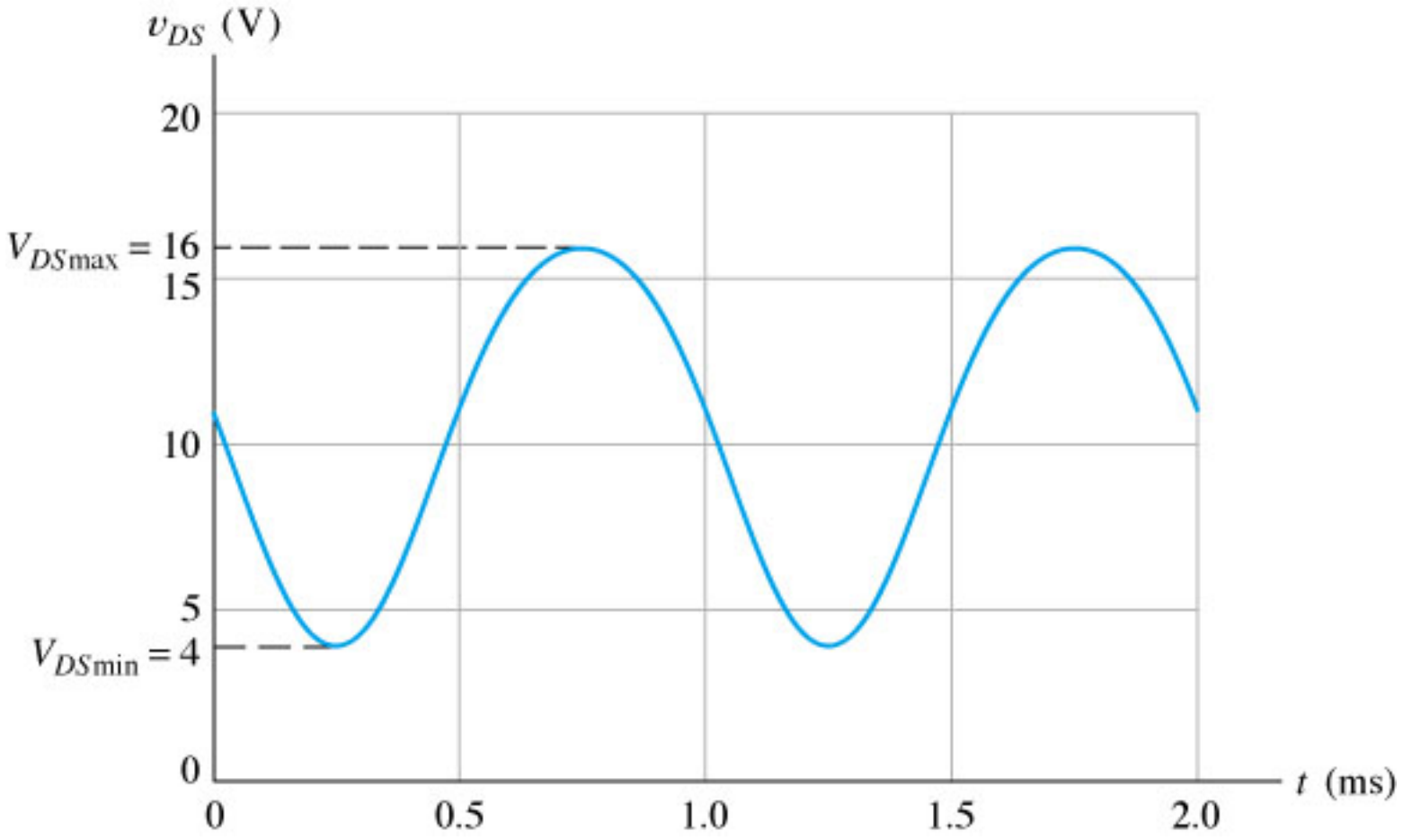



**Figure** $v_{DS}$ versus time for the circuit of Figure 5.13.

# DEPLETION MOSFET

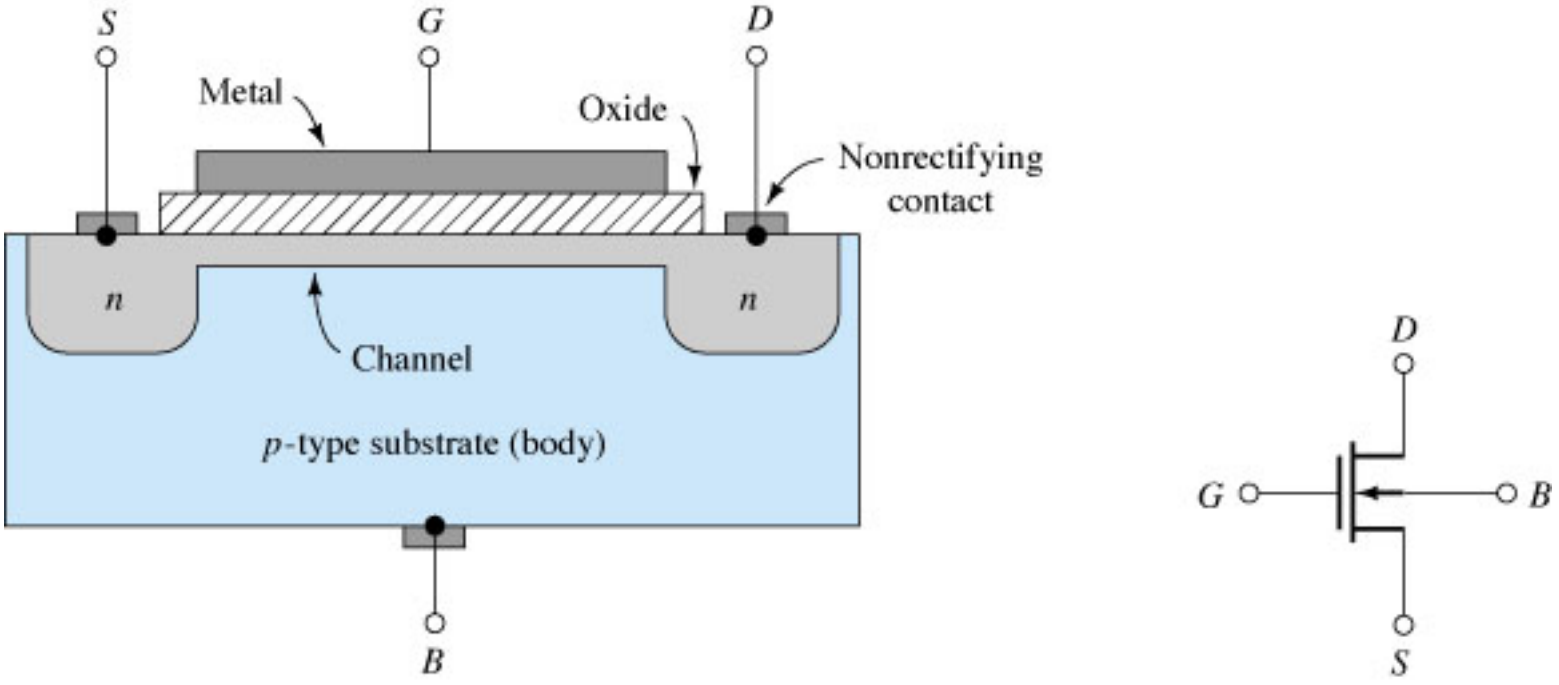



**Figure** *n*-Channel depletion MOSFET.

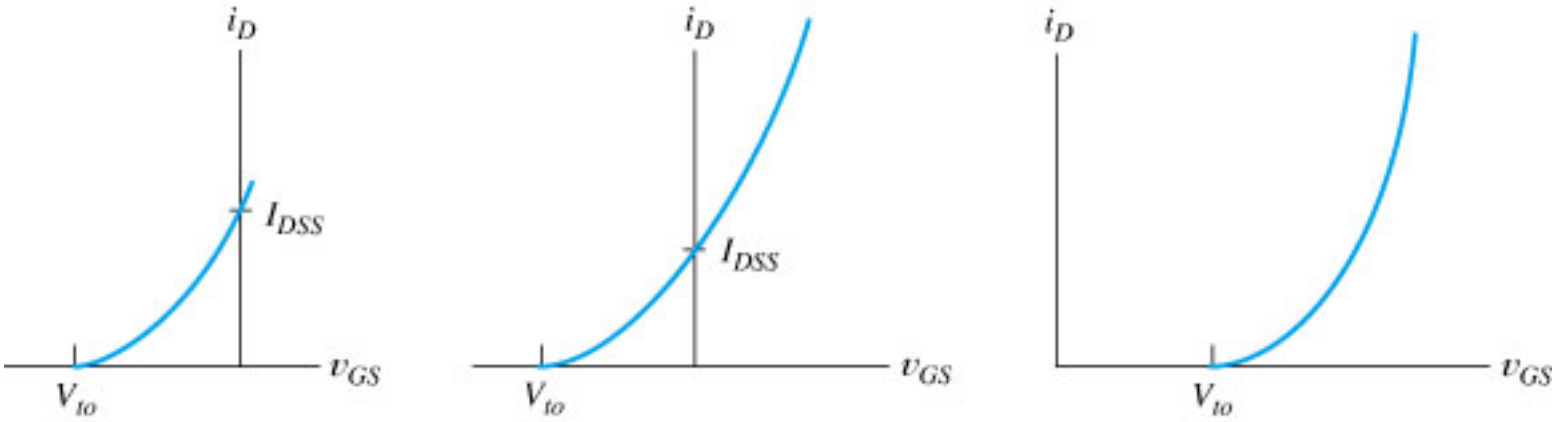



**Figure** Drain current versus $v_{GS}$ in the saturation region for *n*-channel devices.