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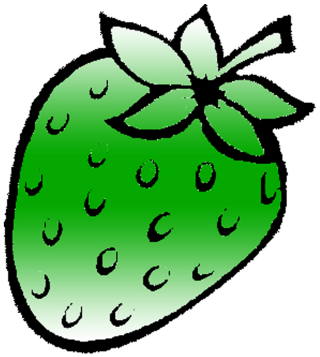

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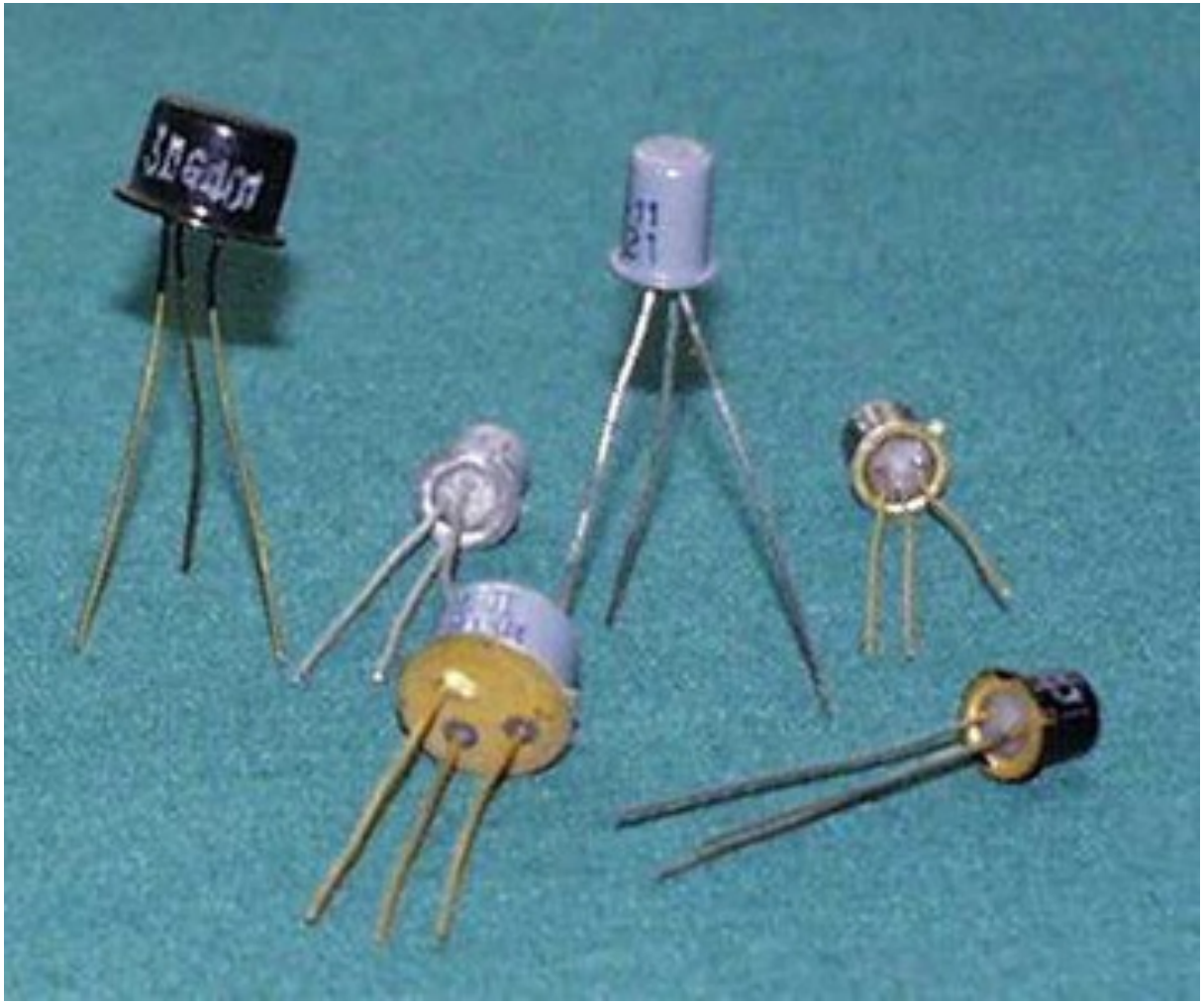
Unit 3
The Bipolar Junction Transistor

Bipolar junction transistors (BJTs)

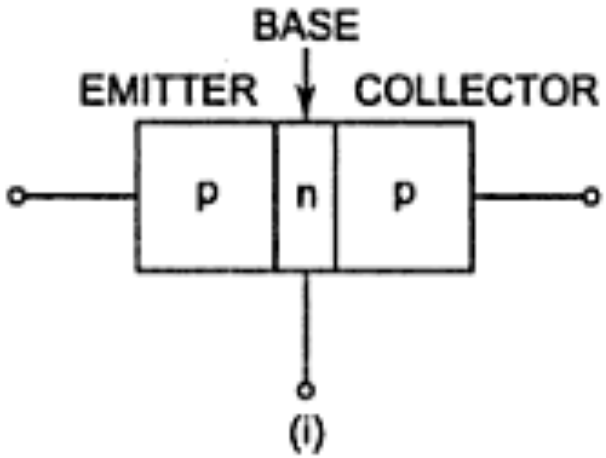


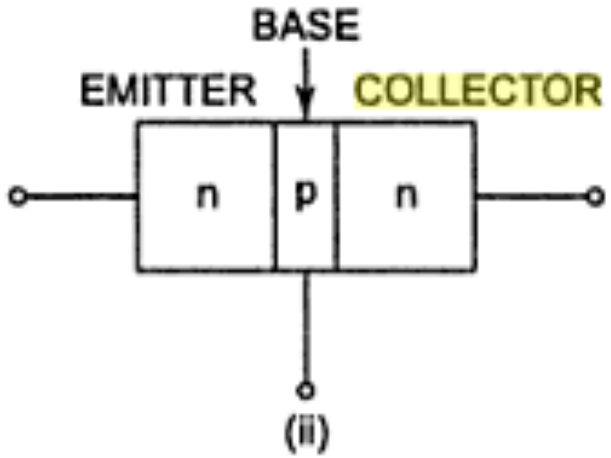
Contents

- Basic Bipolar Junction Transistor,
- Transistor Structures (NPN and PNP)
- Modes of Operation
- Symbol and Conventions
- Current Voltage Characteristics
- Non ideal Transistor
- Leakage current
- Breakdown
- DC analysis of transistor circuit
- CE, CB, CC Configurations
- Basic Transistor action as a switch, as an amplifier
- Transistor Biasing
- Bias Stability
- Different Biasing Circuits
- Understanding Manufacturers Specification

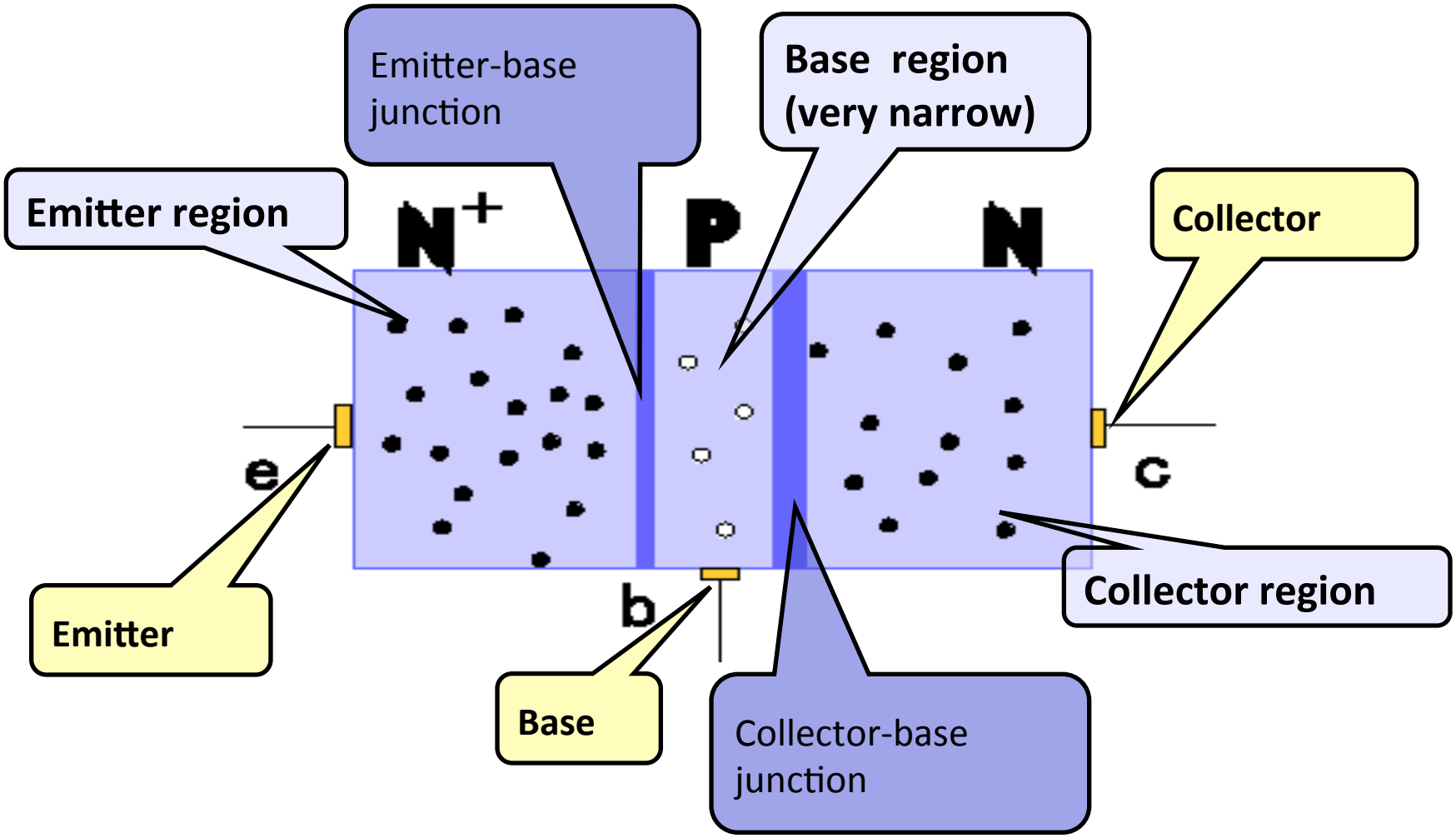
Basic Bipolar Junction Transistor

Transistor Structures

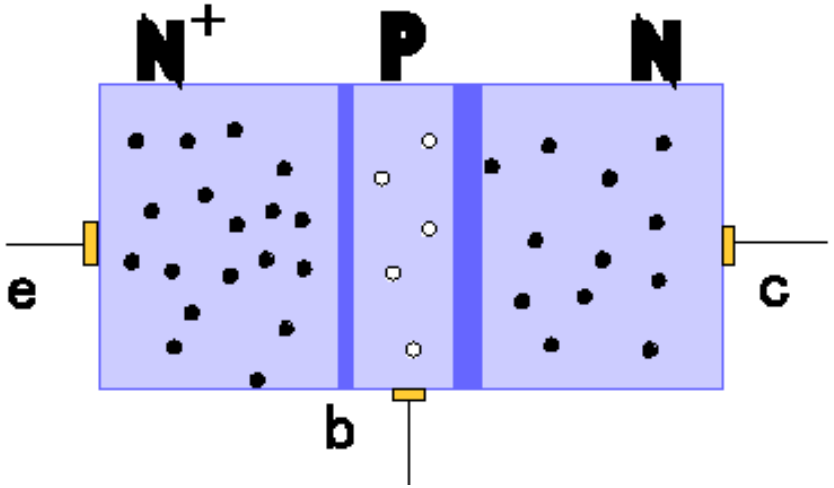




Construction of Bipolar junction transistors



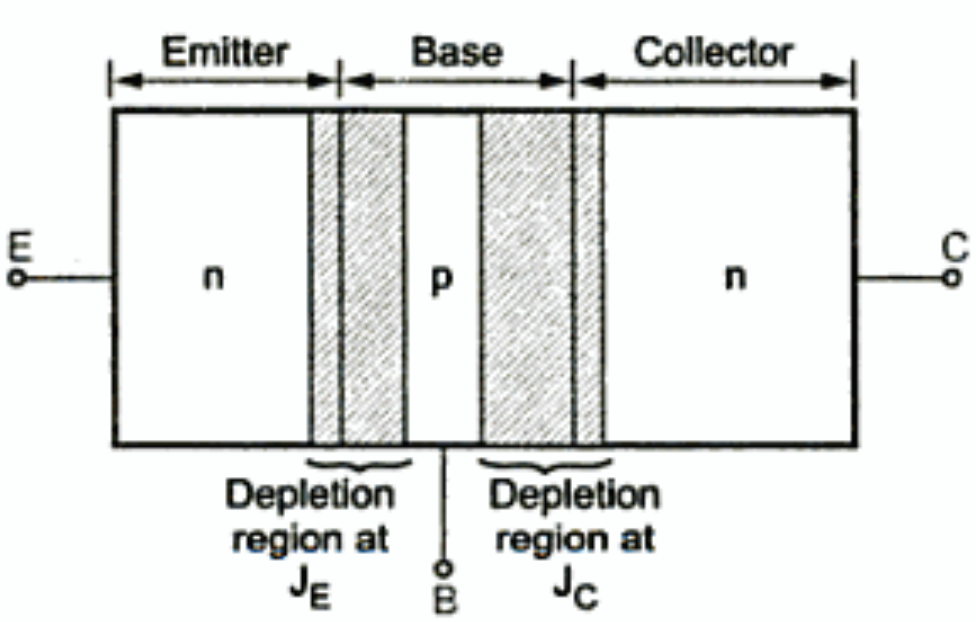
Construction of Bipolar junction transistors



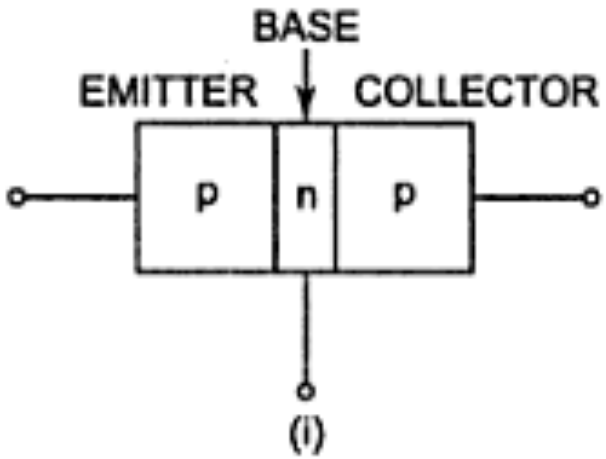
NPN BJT shown

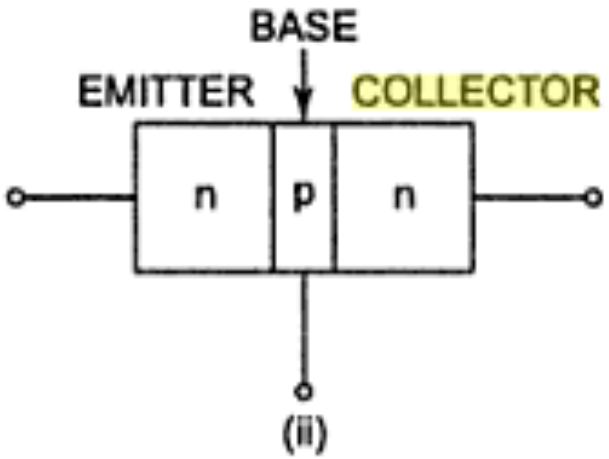
- 3 terminals: emitter, base, and collector
- 2 junctions: emitter-base junction (EBJ) and collector-base junction (CBJ)

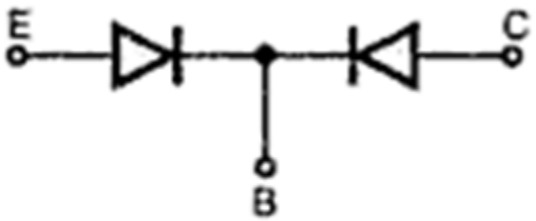
Unbiased npn Transistor



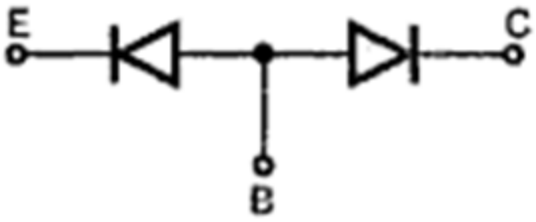
BJT





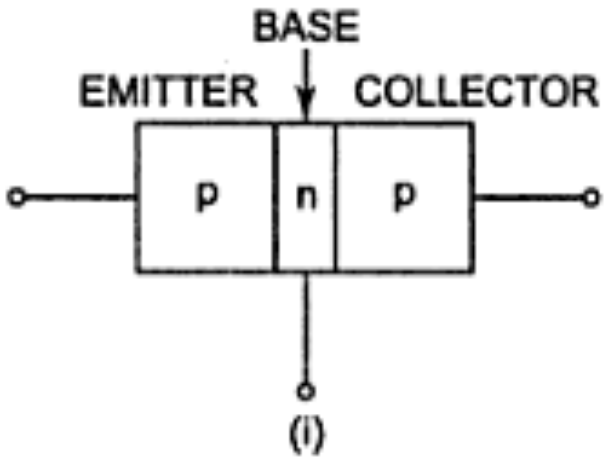


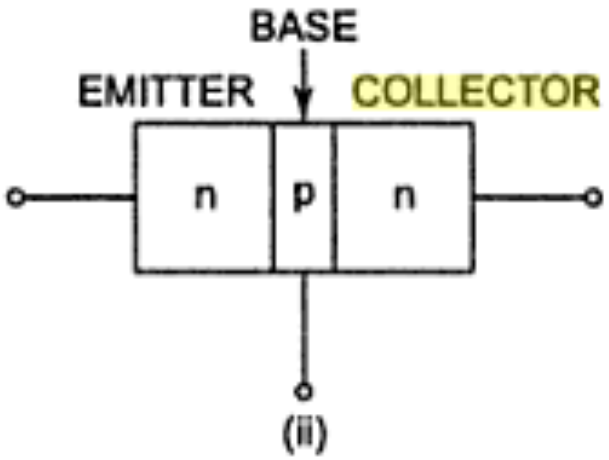
p-n-p transistor

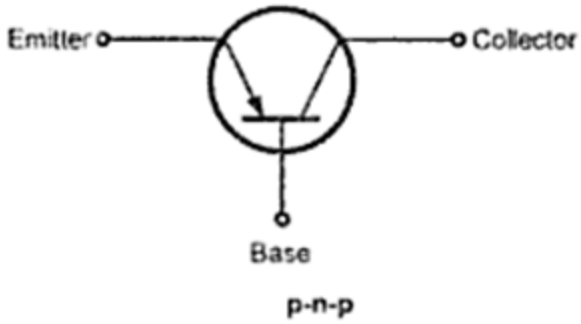


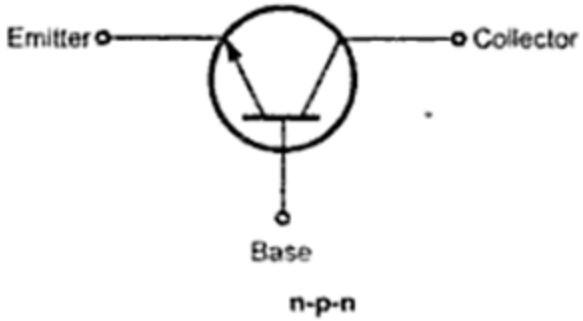
n-p-n transistor

Standard Transistor Symbols









Q: Explain the saturation, cutoff and active modes of transistor

Biased transistor

- Inorder to operate the transistor as an amplifier or switch , the two pn junctions has to be biased properly with external voltages.

- Depending on the external voltage polarity used, the transistor works in one of the three regions.

Region	Emitter base junction	Collector base junction
Active	Forward biased	Reverse biased
Cut-off	Reverse biased	Reverse biased
Saturation	Forward biased	Forward biased

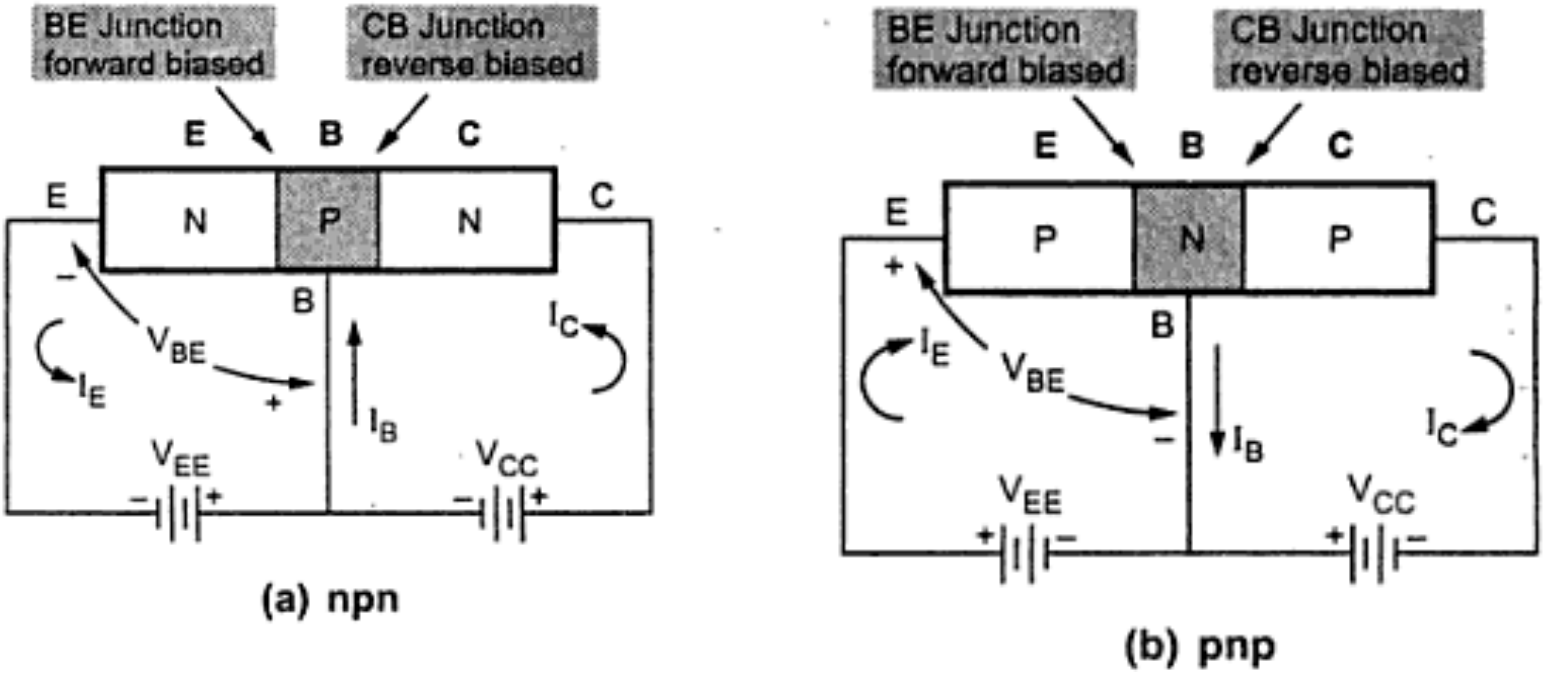
Transistor Biasing

- Transistor as Amplifier – Active Region
- Transistor as ON switch – Saturation Region
- Transistor as OFF switch – Cutoff Region

Working of a npn transistor in Active mode

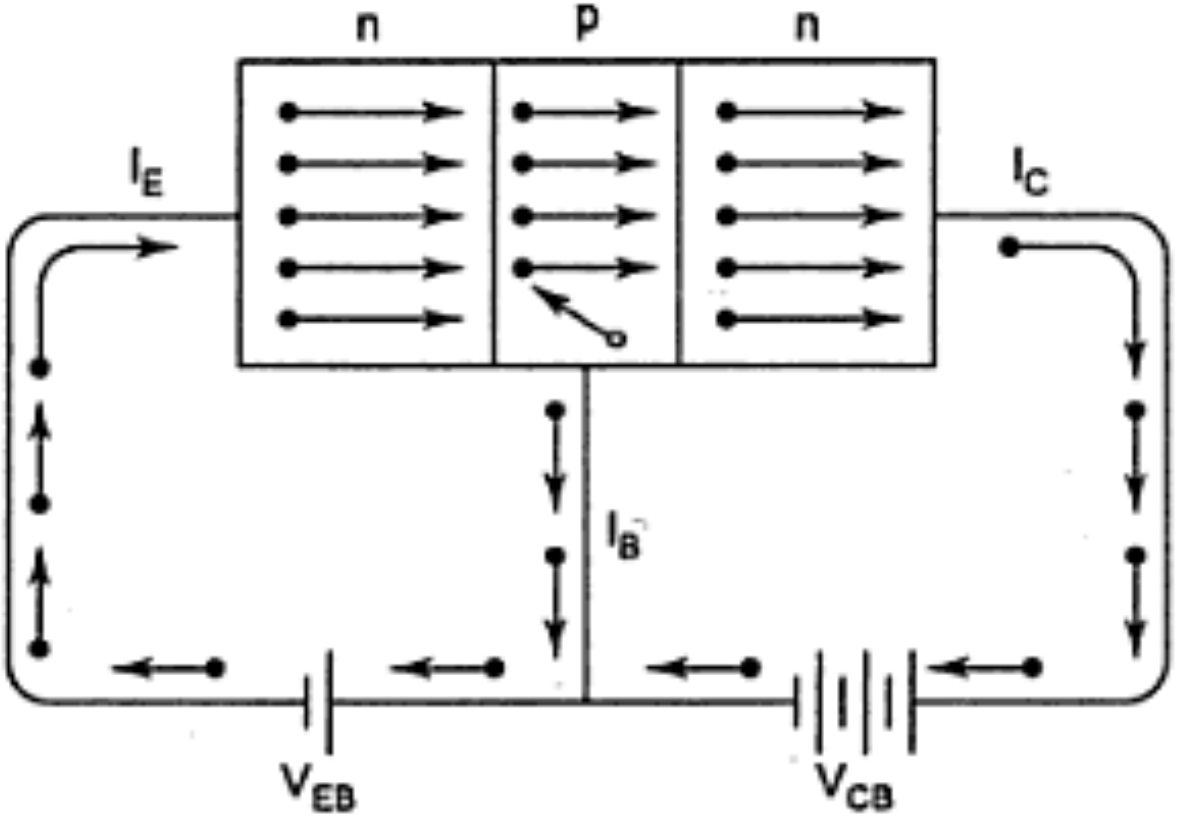
Biased Transistor

Circuit connections for **active region** for npn and pnp transistor



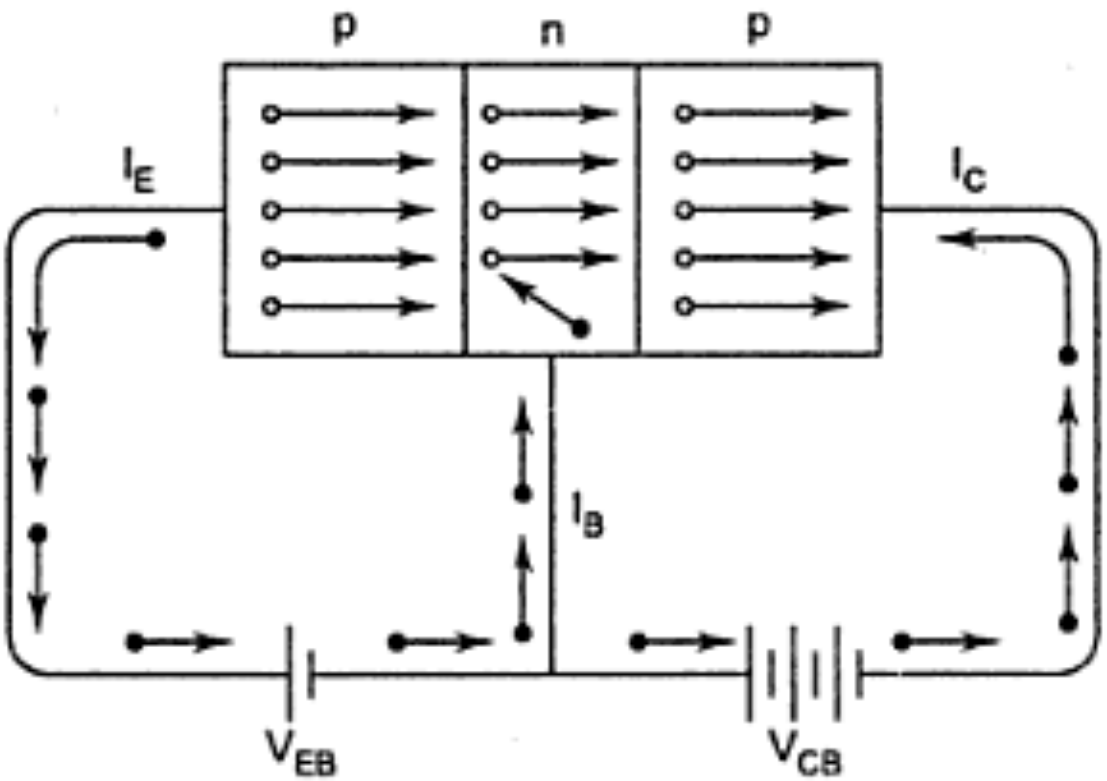
Transistor forward-reverse bias

Working of a npn transistor



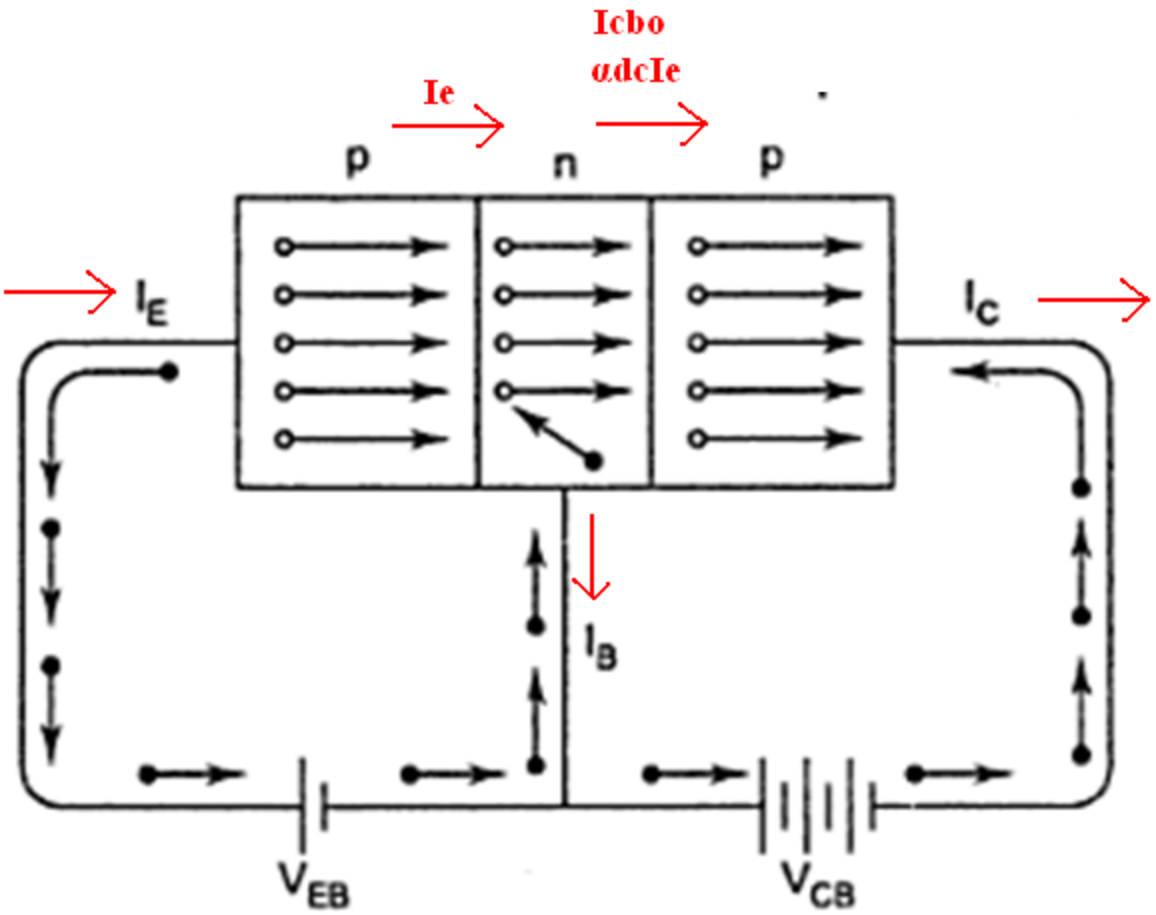
Basic connection of npn transistor

Working of a pnp transistor



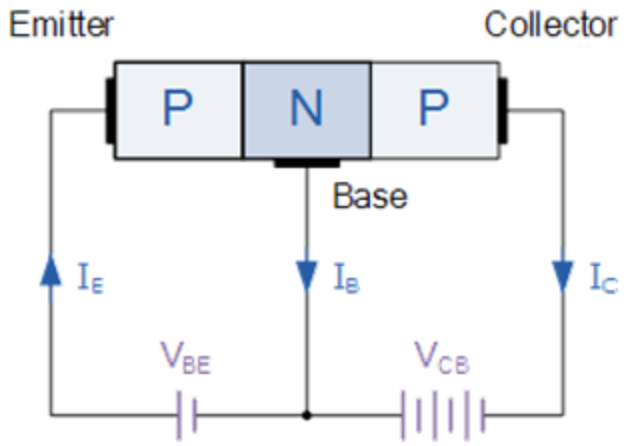
Basic connection of pnp transistor

Transistor Current Relation



Basic connection of pnp transistor

Transistor Current Relation



Relation between different currents in a transistor

The emitter current is equal to the sum of the collector and base currents, *i.e.*,

$$I_E = I_B + I_C$$

$$I_C = \alpha_{dc} I_E$$

α_{dc} is called emitter to collector current gain $\alpha_{dc} = \frac{I_C}{I_E}$

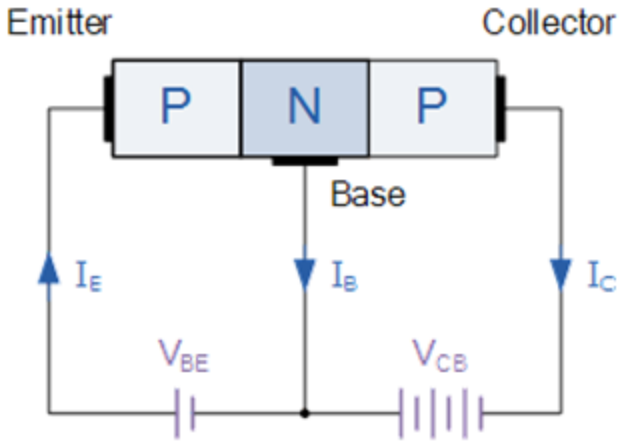
In many circuits , $I_C \approx I_E$, $\alpha_{dc} = 1$

Typical value of α_{dc} = 0.96 to 0.995

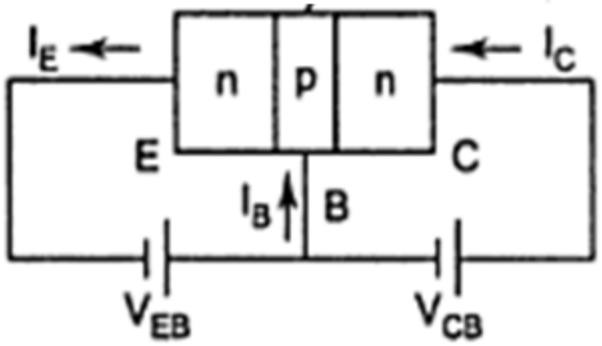
Transistor Current Relation (Cont.)

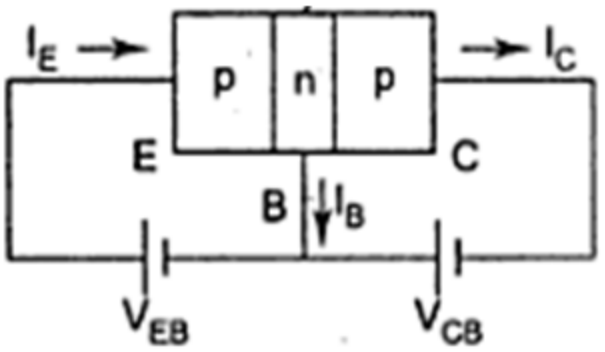
$$I_C = \alpha_{dc} I_E + I_{CBO}$$

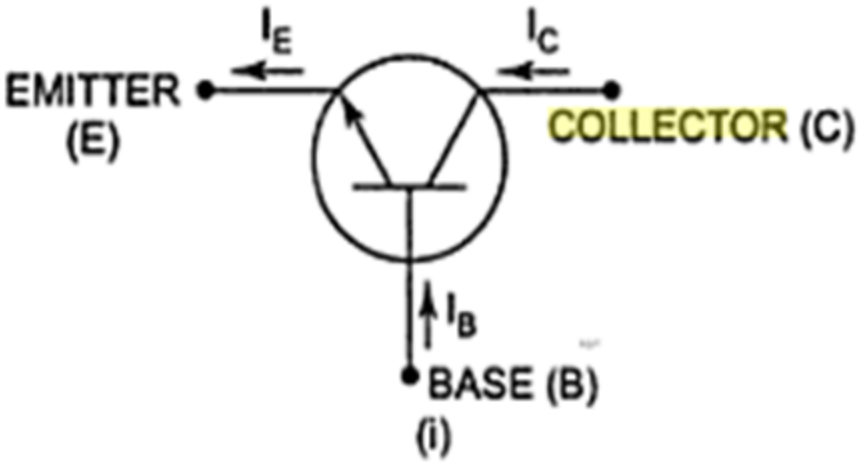
I_{CBO} is called the reverse leakage current which flows as the CB junction is reverse biased.

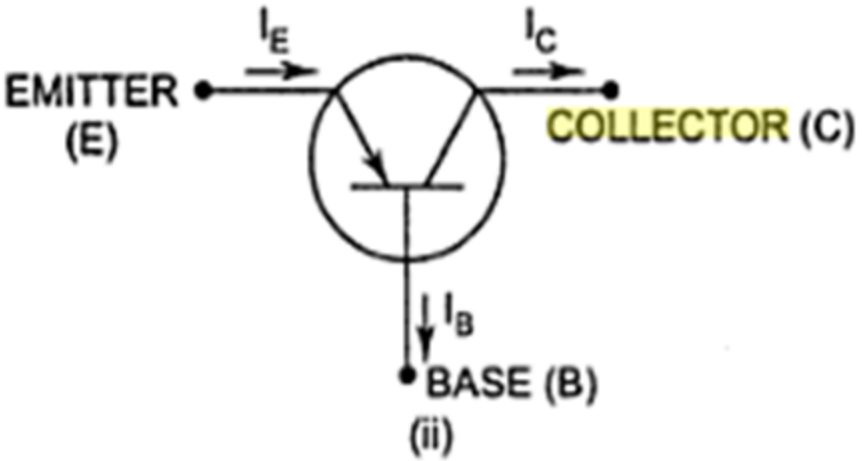


Transistor Current Directions



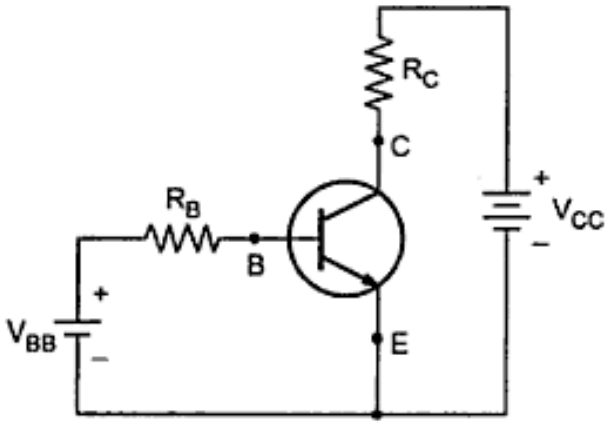




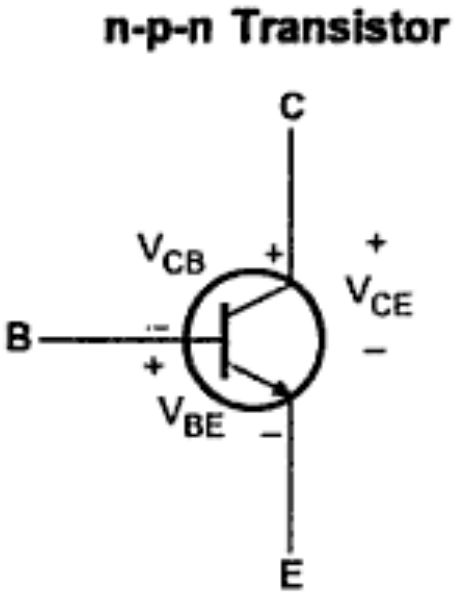


$$I_E = I_B + I_C$$

Transistor Voltage Source Connections and Terminal Voltages



Voltage source connections for n-p-n transistor



Active

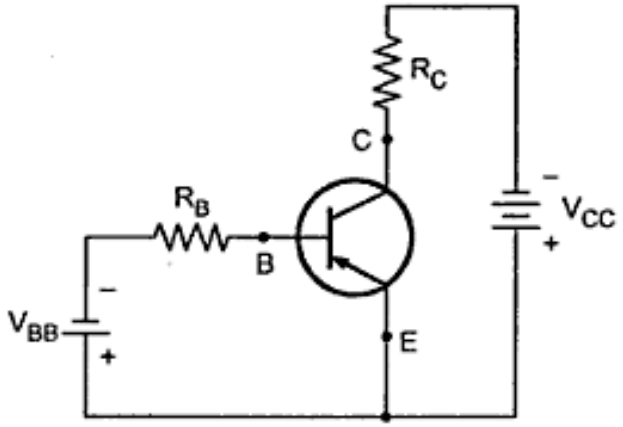
CB junction : Forward Biased

EB junction : Reverse biased

Vcc > Vbb : Active Mode

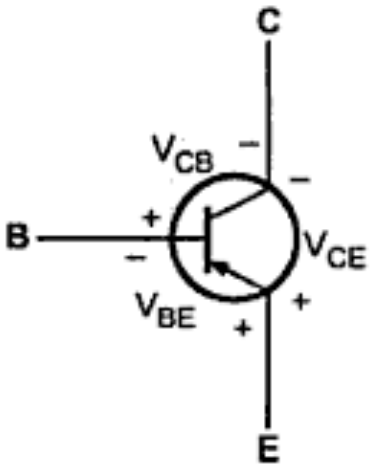
Vcc < Vbb : Saturation mode

Transistor Voltage Source Connections and Terminal Voltages



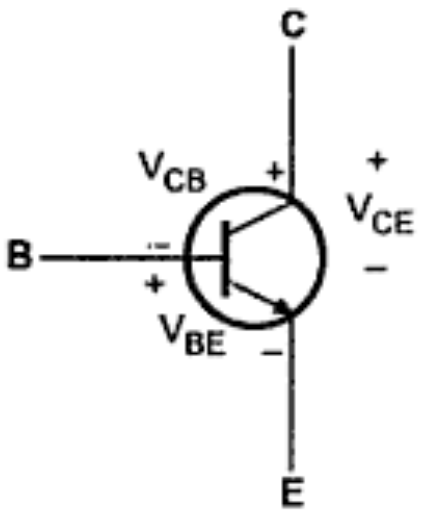
Voltage source connection for p-n-p transistor

PNP Transistor

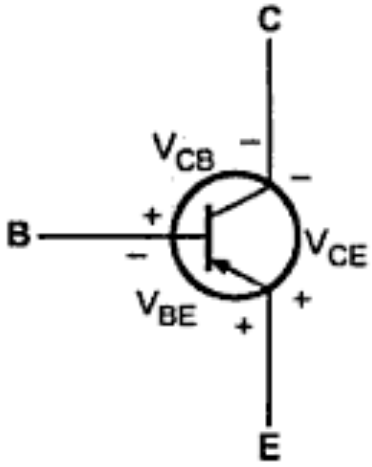


Transistor Voltage Source Connections and Terminal Voltages

n-p-n Transistor



PNP Transistor



$V_{CC} > V_{BB}$ (ACTIVE)

$-V_{CB} - V_{BE} + V_{CE} = 0$

$V_{CB} = V_{CE} - V_{BE}$

$V_{BE} > 0.7$ V

$V_{CE} > 0.7$ V, CB junction is Reverse biased, ACTIVE MODE

$V_{CE} < 0.7$ V, CB junction is Forward biased , SATURATION

Transistor Configurations

DIFFERENT TYPES OF TRANSISTOR CONFIGURATION

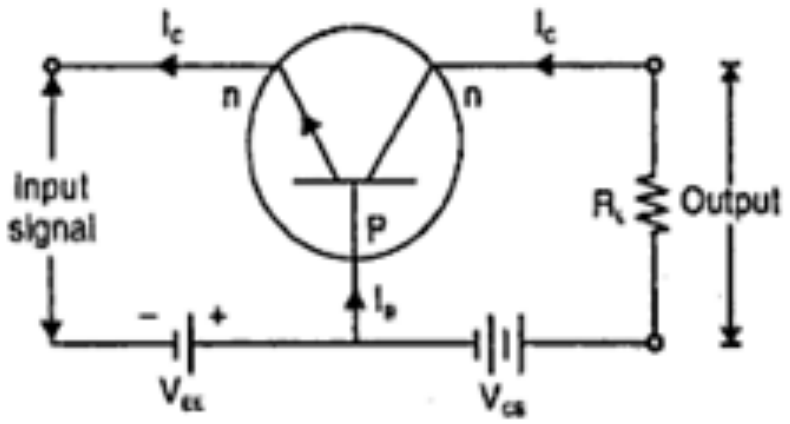
There are three types of transistor configuration possible, namely :

(*i*) Common base (CB) configuration

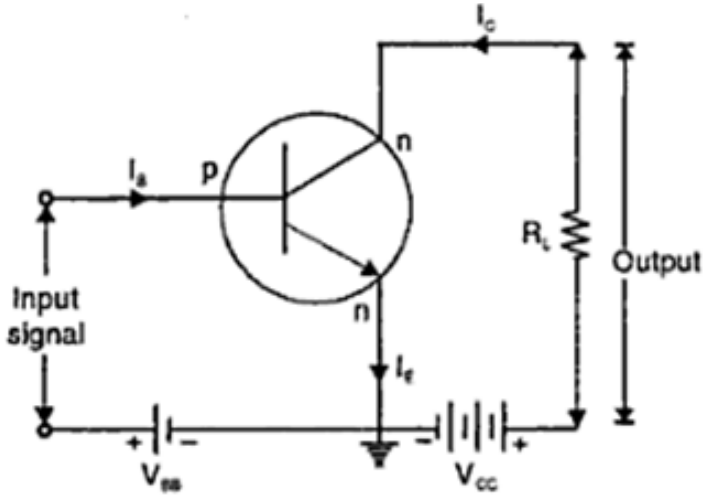
(*ii*) Common emitter (CE) configuration

(*iii*) Common collector (CC) configuration

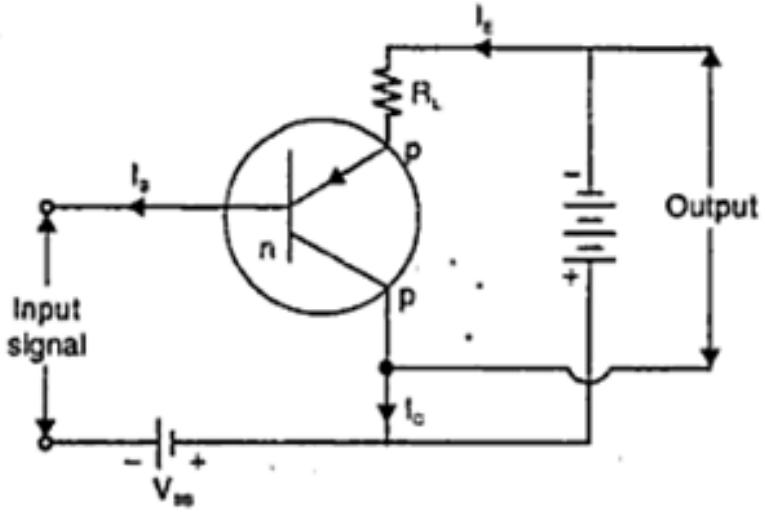
Transistor Configurations



(*a*) Common base configuration with *npn* transistor



(*a*) Common emitter circuit of *npn* transistor



(*b*) Common collector circuit of *pnp* transistor

Transistor Characteristic

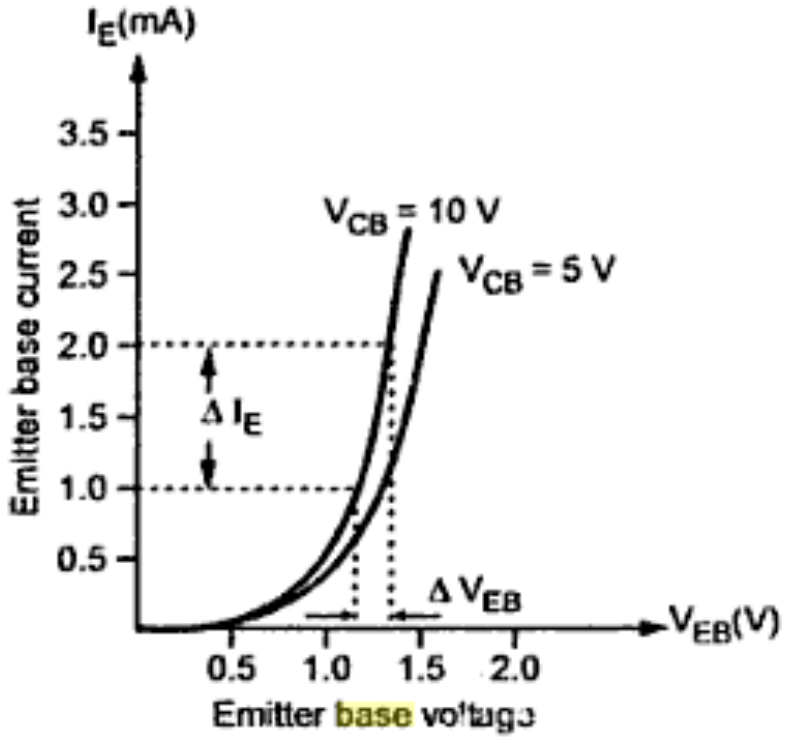
Characteristic of CB

There are two important characteristics of CB. Configuration namely :

(1) Input characteristics.

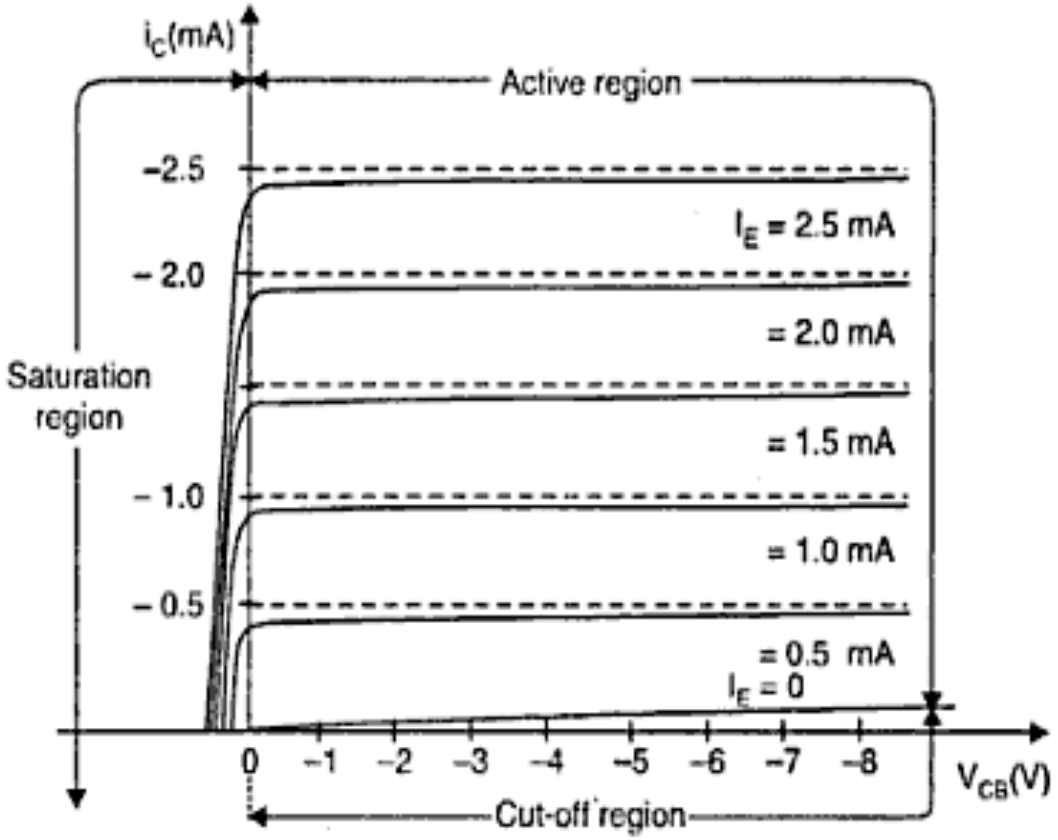
(2) Output characteristics.

Input Characteristic



Input characteristics of transistor in CB configuration

Output Characteristic



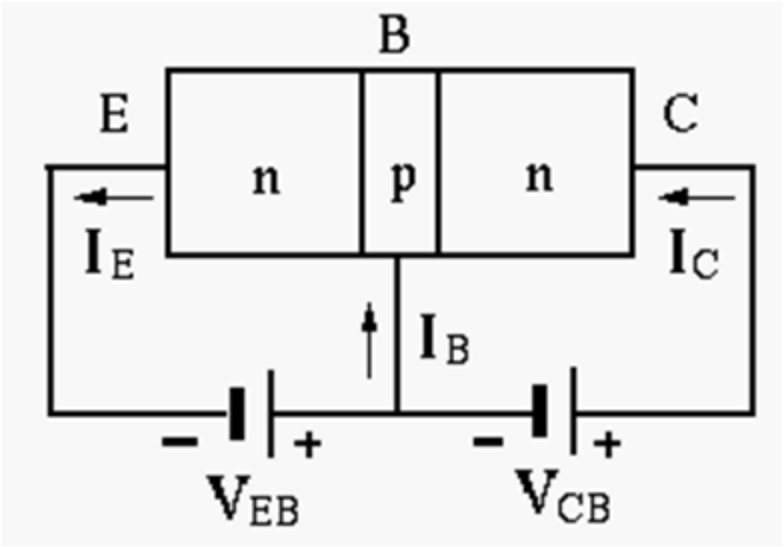
Operating Regions

- Active Region
- Cutoff Region
- Breakdown Region
- Saturation Region

Parameters

- Dynamic Input Resistant (r_i)
- Dynamic Output Resistance (r_o)
- Dc current gain (α_{dc})
- Short Circuit Current Gain (α or h_{fb})

COMMON BASE CONFIGURATION



Emitter current amplification factor (α)

$$\alpha = \frac{\Delta I_C}{\Delta I_E} \quad \text{at constant } V_{CB}$$

$$I_E = I_C + I_B$$

or $\Delta I_E = \Delta I_C + \Delta I_B$,

CB *current gain* or *current transfer ratio*:

$$\alpha = \frac{I_C}{I_E} < 1$$

For example, α = 0.99, indicates that 99%of the electrons from the emitter arrive at the collector to form Ic while only 1% combined with the hole in the base to form I_B

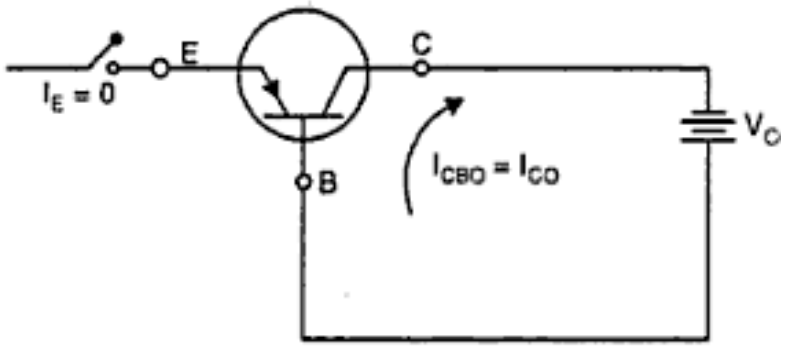
Total collector current of a common base (CB) configuration

total collector current

$$I_C = \alpha\ I_E + I_{leakage}$$

$$I_C = \alpha\ I_E + I_{CBO}$$

Here, I_{CBO} (leakage current) is due to minority charge carriers *i.e.*, collector base junction open emitter (or $I_E = 0$).



Reverse leakage current in CB configuration.

Common Base Configuration

The relationship between the output I_C and the input I_E can be found as:

$$I_C = \alpha I_E + I_{CB0} \approx \alpha I_E$$

The base current I_B is:

$$I_B = I_E - I_C \approx I_E - \alpha I_E = (1 - \alpha) I_E$$

Summary :

$$\begin{cases} I_C = \alpha I_E \\ I_B = I_E - I_C = (1 - \alpha) I_E \end{cases}$$

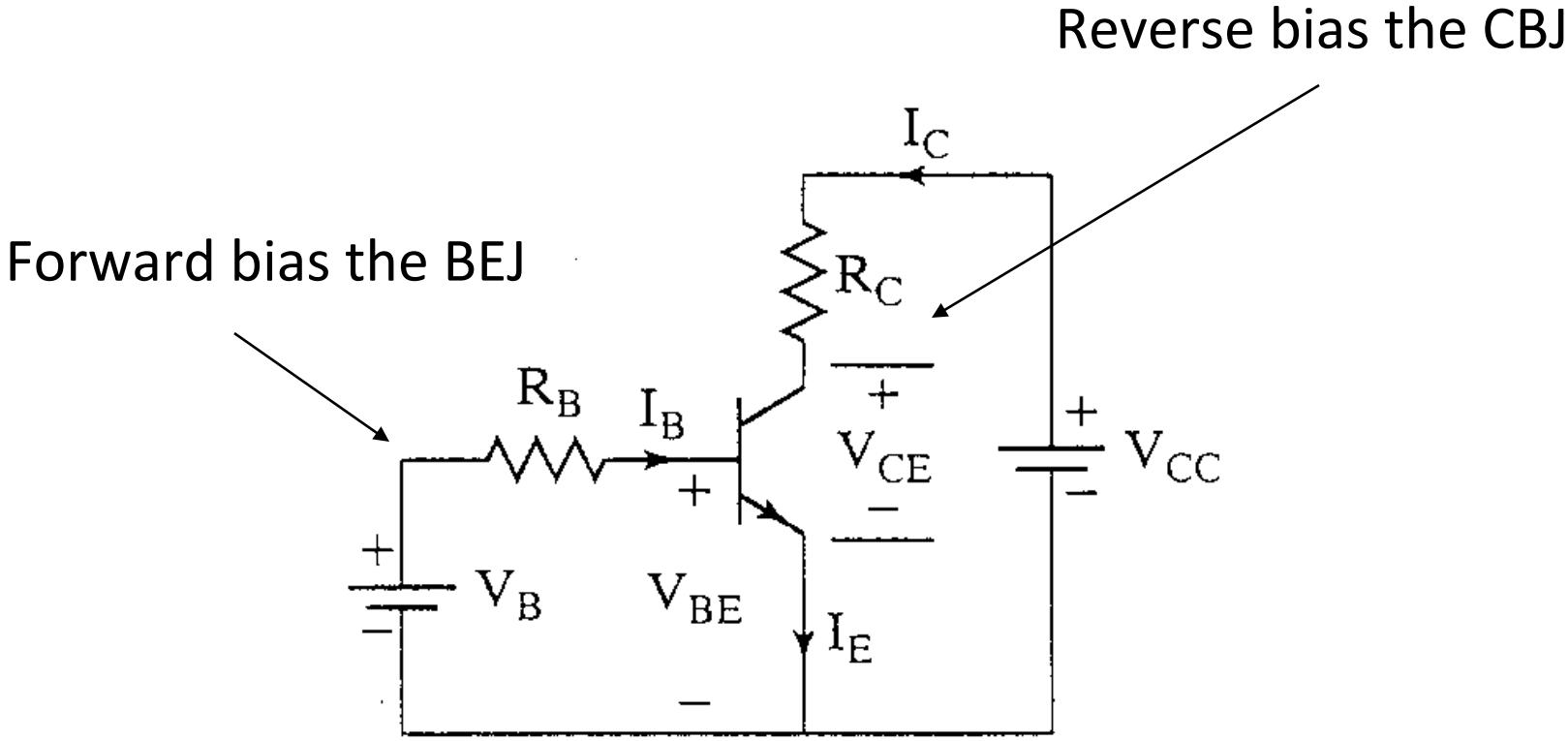
Characteristic of CE

There are two important characteristics of CE configuration namely :

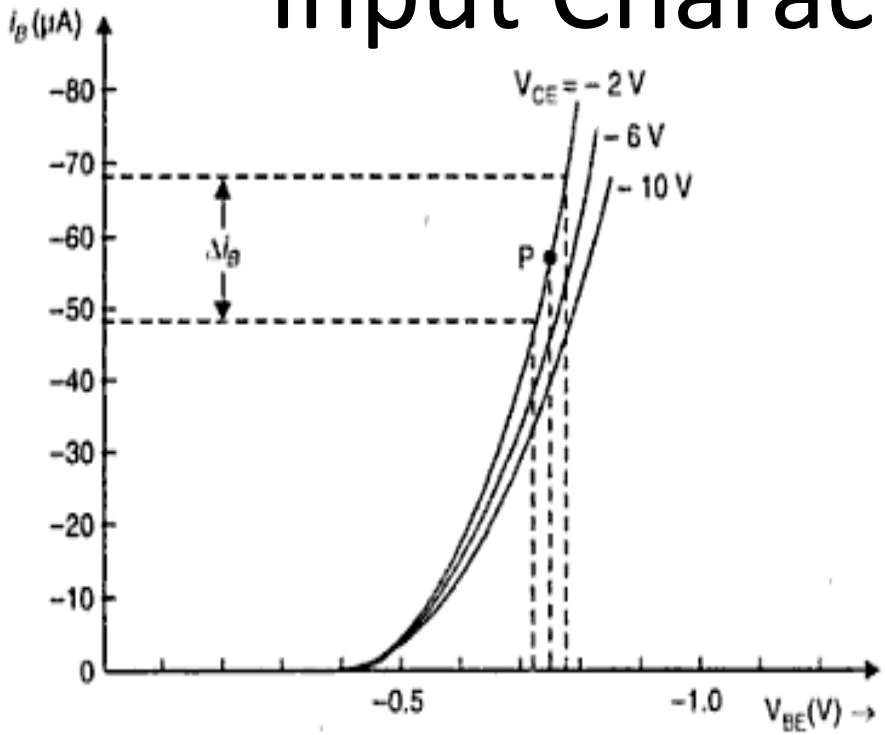
(1) Input characteristics.

(2) Output characteristics.

Common-Emitter NPN Transistor

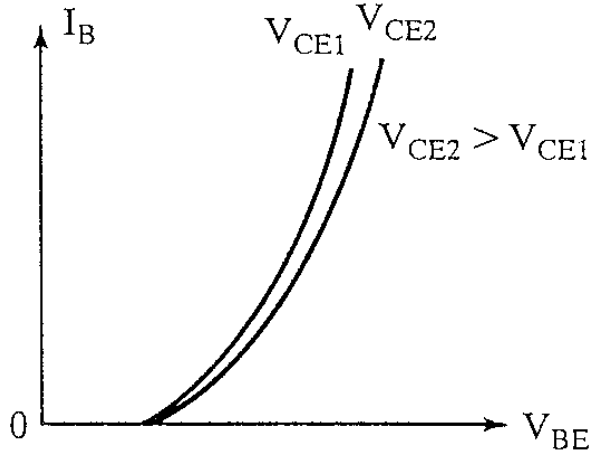


Input Characteristic of CE



Common-emitter input characteristics of a PNP transistor.

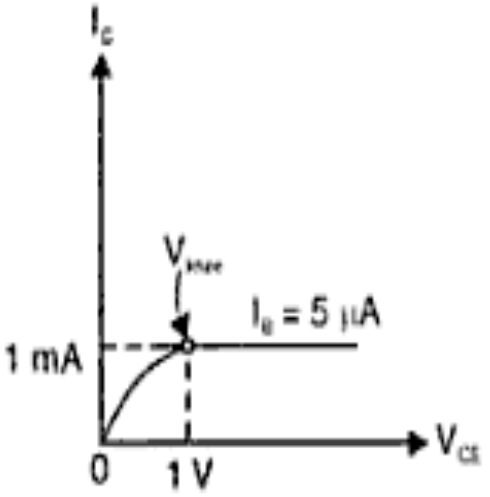
- Plot I_B as f(V_{BE}, V_{CE})
- As V_{CE} increases, more V_{BE} required to turn the BE on so that I_B>0.
- Looks like a pn junction volt-ampere characteristic.



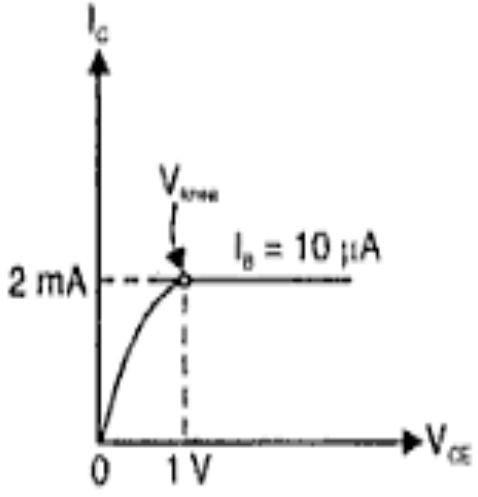
Input Resistance.

$$r_i = \frac{\Delta V_{BE}}{\Delta I_B} \text{ at constant } V_{CE}$$

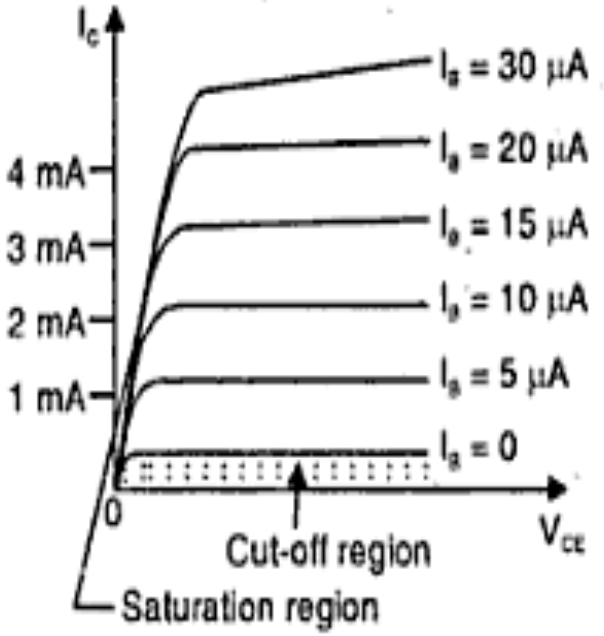
Output Characteristic of CE



(i)



(ii)



(iii)

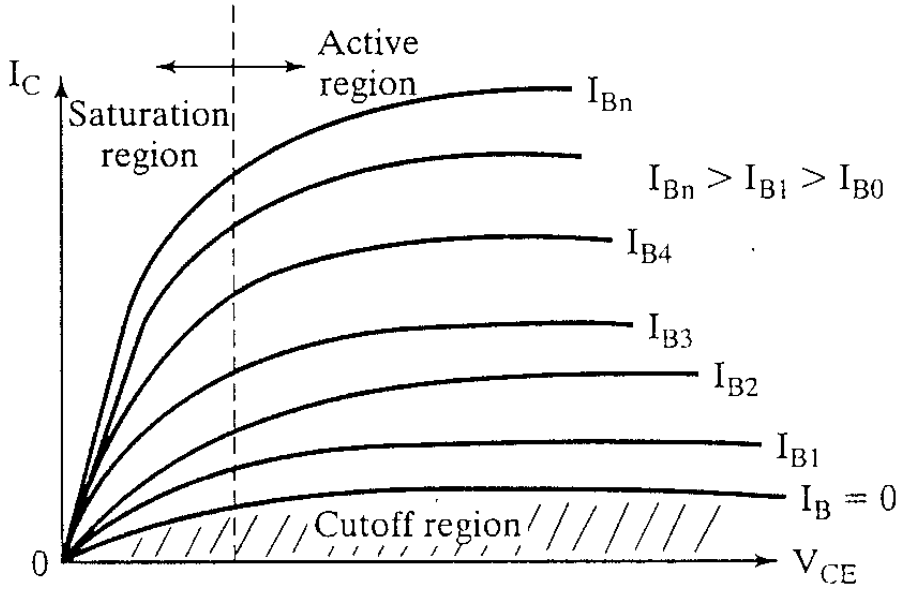
Output resistance.

Output resistance, $r_o = \dfrac{\Delta V_{CE}}{\Delta I_C}$ at constant I_B

Output Characteristics

Q : Explain the three regions of operation of CE BJT

- Plot I_C as f(V_{CE}, I_B)
- Cutoff region (off)
  - both BE and BC reverse biased
- Active region
  - BE Forward biased
  - BC Reverse biased
- Saturation region (on)
  - both BE and BC forward biased



CE Configuration

Base current amplification factor (β)

$$\beta = \frac{\Delta I_C}{\Delta I_B} = \frac{\text{Variation in collector current}}{\text{Variation in base current}}$$

Relation between α and β

Q : Derive the relation between α and β hence find the value of β if α = 0.95

We know that

$$\alpha = \frac{\Delta I_C}{\Delta I_E}$$

$$\beta = \frac{\Delta I_C}{\Delta I_B}$$

$$\Delta I_E = \Delta I_C + \Delta I_B$$

$$\frac{\Delta I_E}{\Delta I_C} = \frac{\Delta I_C}{\Delta I_C} + \frac{\Delta I_B}{\Delta I_C}$$

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta}$$

$$\boxed{\beta = \frac{\alpha}{1 - \alpha}}$$

Therefore, above relation shows that as α approaches to unity, β approaches to infinity. In other words, the current gain in common emitter configuration is very high.

Q : Find the value of α if β of the transistor is 49.

Find the value of Ic of the transistor using both α and β rating of the transistor

$$\alpha = \frac{\beta}{1 + \beta}$$

$$\alpha = \frac{49}{1 + 49} = .98$$

$$I_C = \alpha\ I_E = .98\ (12\ \text{mA}) = 11.76\ \text{mA}$$

$$I_C = \beta\ I_B = 49\ (240\ \mu\text{A}) = 11.76\ \text{mA}.$$

Q : A certain transistor has α=.98 , Ico = 5 μA, I_B = 100 μA. Find the values of collector current and emitter current.

Solution : Given $\alpha = .98$

$I_{CO} = 5\ \mu A$

$I_B = 100\ \mu A$

We know that the collector current given by the relation,

$$I_C = \beta\ I_B + (1 + \beta)\ I_{CO} \text{ and}$$

From relation, $$\beta = \frac{\alpha}{1 - \alpha} = \frac{.98}{1 - .98} = 49.$$

Then $$I_C = 49.100 \times 10^{-6} + (1 + 49)\ 5 \times 10^{-6}$$

$$= 4900 \times 10^{-6} + 250 \times 10^{-6}\ A$$

$$= 5150 \times 10^{-6}\ A$$

$$= 5.150\ mA \quad \textbf{Ans.}$$

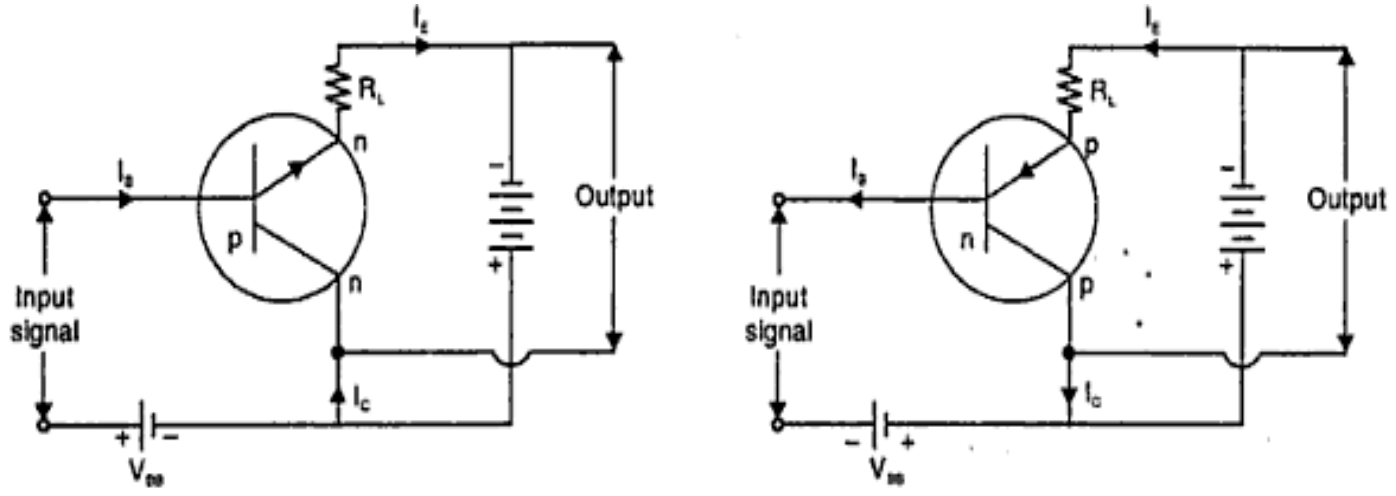
Also we know that the emitter current

$$I_E = I_C + I_B$$

$$I_E = 5.150\ mA + 100\ \mu A$$

$$I_E = 5.25\ mA.$$

Common Collector (CC) Configuration



(a) Common collector circuit of *npn* transistor

(b) Common collector circuit of *pnp* transistor

Current amplification factor (γ)

$$\gamma = \frac{\Delta I_E}{\Delta I_B}$$

Q : Derive the relation between α and β hence find the value of β if α = 0.95

Relation between γ and α

We know that

$$\alpha = \frac{\Delta I_C}{\Delta I_E}$$

$$\boxed{\gamma = \frac{\Delta I_E}{\Delta I_B}}$$

$$\Delta I_E = \Delta I_C + \Delta I_B$$

$$\boxed{\gamma = \frac{1}{1 - \alpha}}$$

Comparison of the configurations

Parameters	*C-B configurations*	*C-E configuration*	*C-configuration*
1. Input dynamic resistance	Very low (20 Ω)	Low (1 KΩ)	Very high (1 MΩ)
2. Output dynamic resistance	Very high (1 MΩ)	High (10 KΩ)	Very low (25 Ω)
3. Current gain	Less than unity	Large (50 to 100)	Very high (150)
4. Voltage gain	Very high (150)	Large (100 to 125)	Less than unity.

CE Configuration widely used in amplifier circuit ?

CE Configuration is mostly used due to :

- High Voltage Gain
- High Current Gain
- High Power Gain

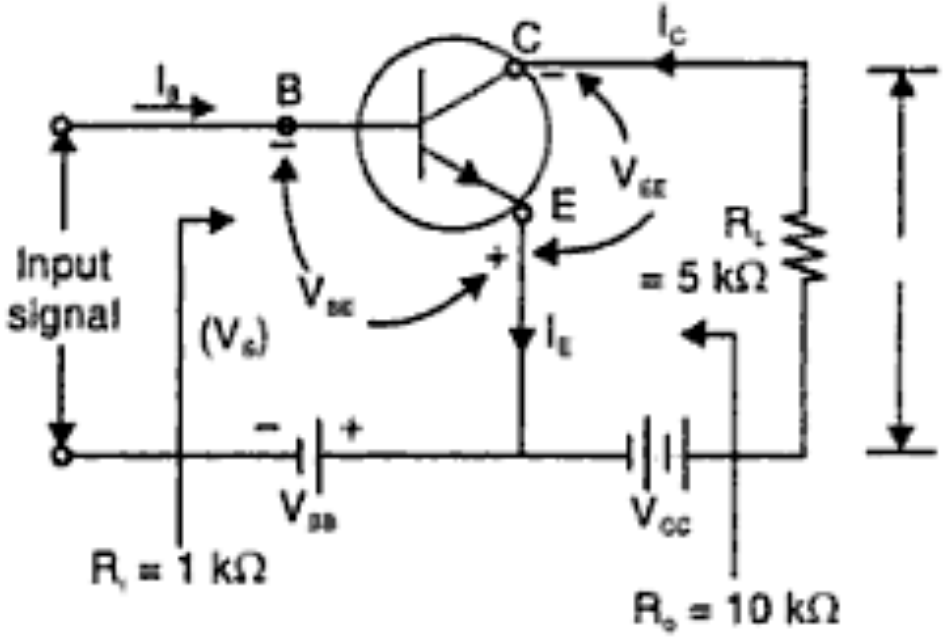
Q: With the help of neat diagram, explain the construction , characteristics and working of typical BJT used for voltage amplification

Ans: (points)

Construction of Transistor.
Transistor as an amplifier uses active mode of biasing.
Active mode of biasing – Emitter Base junction is Forward Biased and Collector Base junction is Reverse Biased .
Transistor configuration used for amplifier is Common Emitter configuration.
Draw the circuit diagram.
Draw the output characteristic of Transistor in CE mode and explain the working

Transistor as an amplifier

Q: Draw and Explain the Transistor as an amplifier

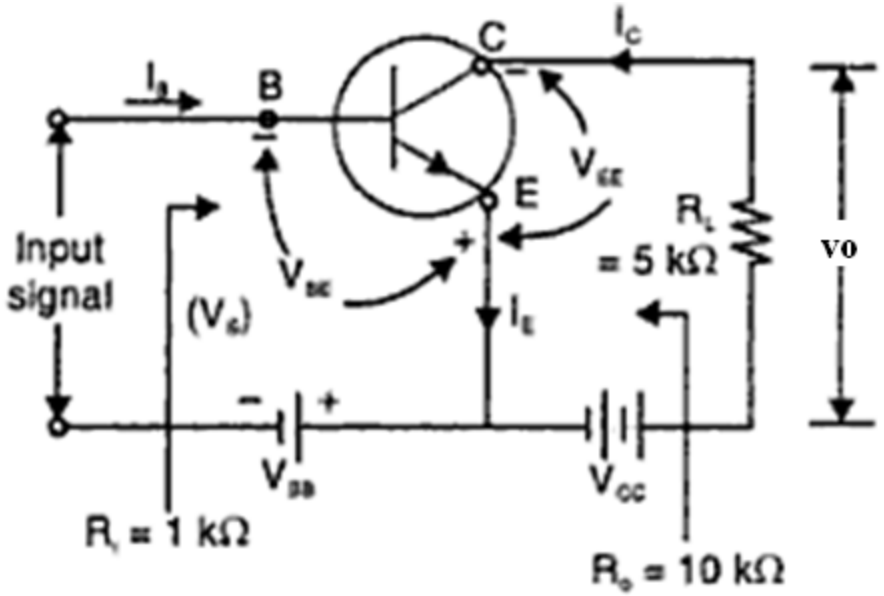


A basic transistor amplifier in common-base configuration.

A signal source Vs is connected in input circuit.

Input impedance of the transistor is 1KΩ, output impedance is 10KΩ.

Q: Draw and Explain the Transistor as an amplifier



Signal Vs is superimposed on dc voltage V_{BB}

V_{BE} varies with time.

I_B varies with time as a result collector current I_c and emitter current I_E varies with time.

This varying , collector current I_c passes through R_L and a varying output voltage is developed across it.

Example:

To understand how a signal voltage is magnified

Input signal voltage Vs = 20 mV (rms)

Input impedance of the transistor is 1KΩ, output impedance is 10KΩ.

$$I_B = \frac{20 \times 10^{-3}}{1 \times 10^{3}} = 20\ \mu A$$

Dc current gain of transistor (β) of CE transistor is 100

$$I_C = \beta\ I_B = 100 \times 20\ \mu A = 2\ mA$$

Output resistance of transistor is very high,

therefore output voltage Vo is approximately:

$$V_0 = I_C\ R_L = 2\ mA \times 5\ k\Omega = 10\ V$$

Q: Draw and Explain the Transistor as an amplifier

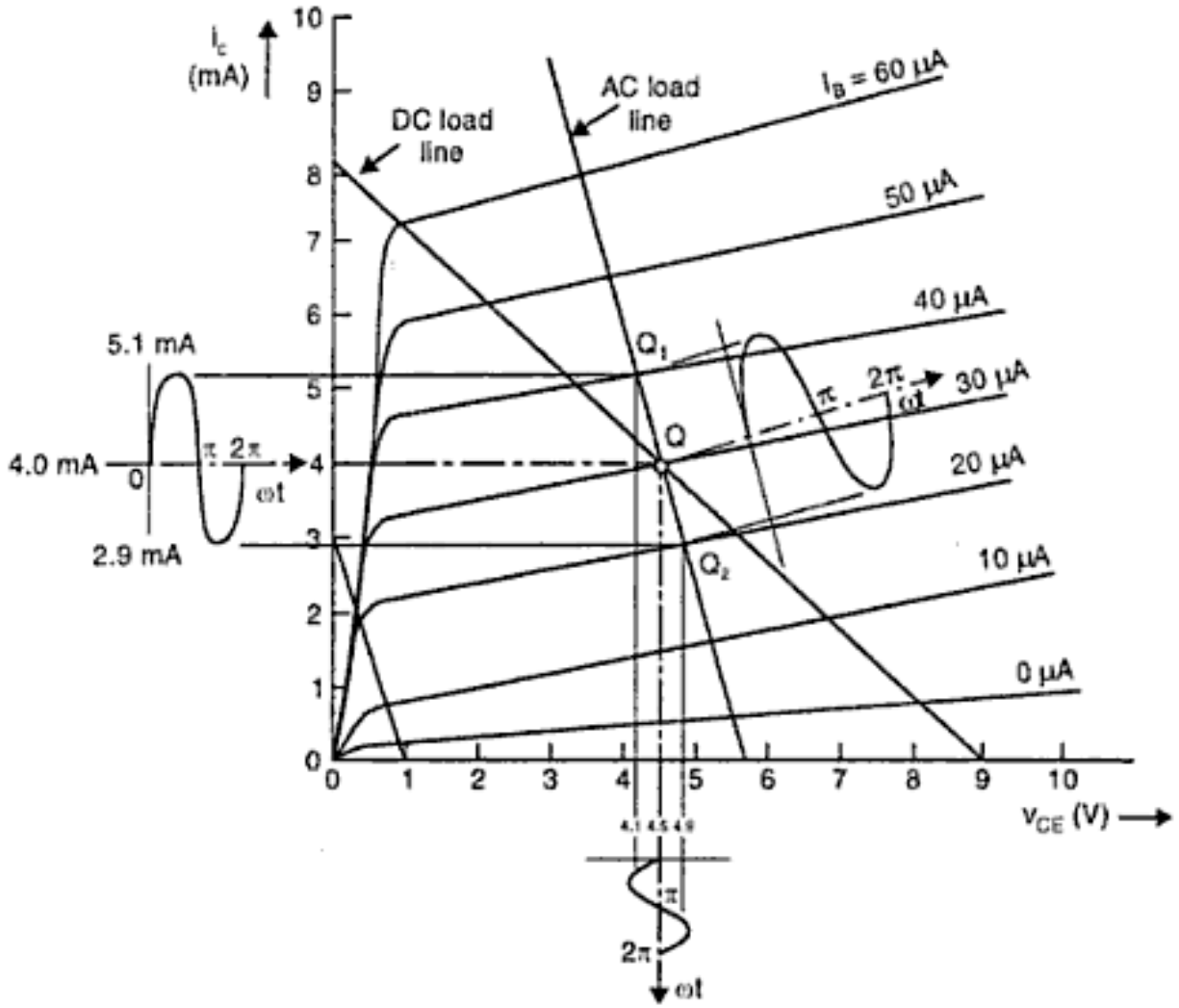
Voltage Amplification :

$$A_V = \frac{V_0}{V_S} = \frac{10}{20\ \text{mV}} = 500$$

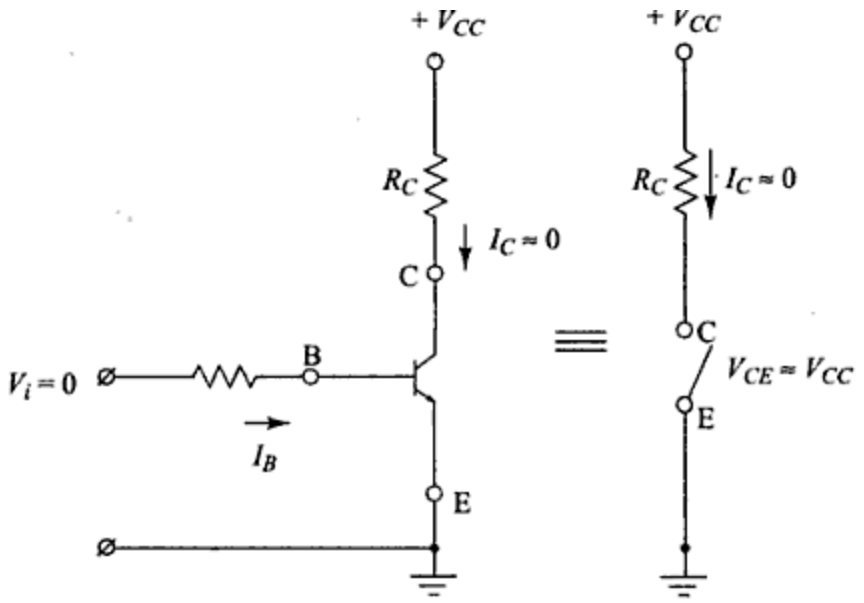
Thus, Transistor Amplifying action is basically due to its capability of transferring its signal current from low resistance circuit to a high resistance circuit

Transfer + Resistor = TRANSISTOR

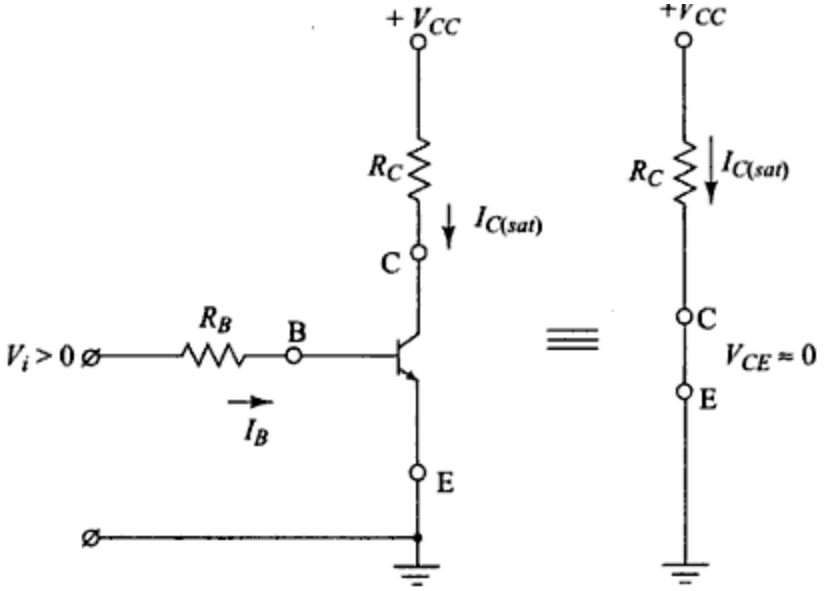
Graphical method



Transistor as a Switch



(a) npn transistor (open switch)



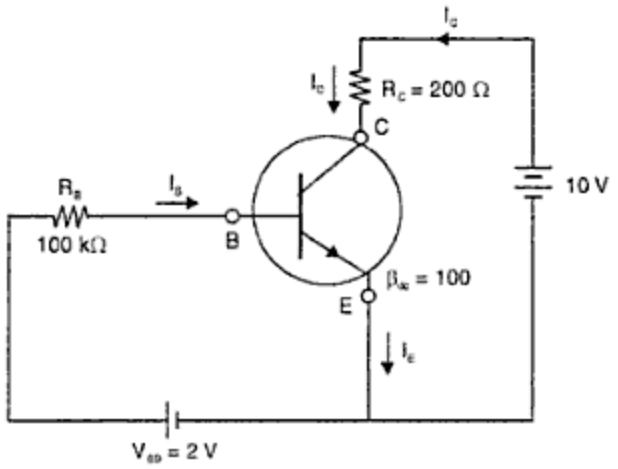
(b) npn transistor (closed switch)

Switch condition	I_C		V_{CE}	
	Ideal	*Practical*	*Ideal*	*Practical*
OFF	0	I_{CO}	Open circuit	Maximum V_{CC}
ON	∞	$I_{C(sat)}$	0	$V_{CE(sat)}$

Operating Point

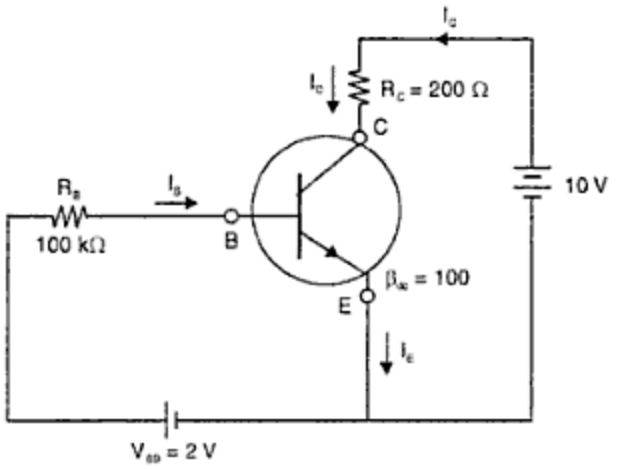
Values of V_{CE} and I_c in the absence of ac input signal (V_s) is called OPERATING POINT

OPERATING POINT = (I_c ,V_{CE}) values of the given circuit with the applied DC bias for no input signal



CE-Configuration circuit.

Example: To find operating point for the given circuit.



CE-Configuration circuit.

Applying KVL to the input section and neglecting V_{BE}

$$V_{BB} = R_B\ I_B$$

$$I_B = \frac{V_{BB}}{R_B} = \frac{2}{10} = .2\ \text{mA}$$

$$I_C = \beta\ I_b = 100 \times .2 = 20\ \text{mA}$$

Contd:

Applying KVL to the output section:

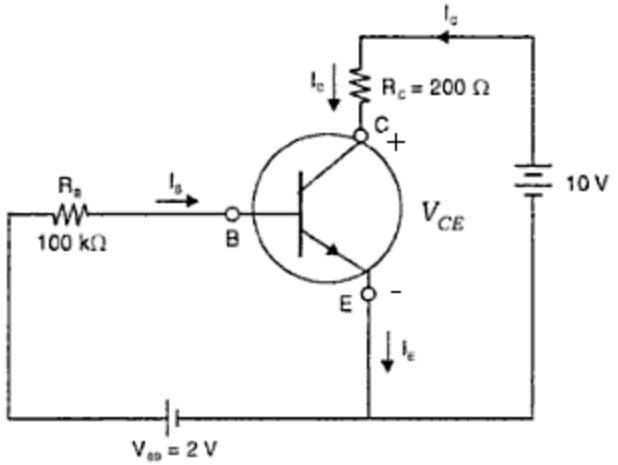
$$V_{cc} - I_c R_c - V_{cE} = 0$$

$$V_{CE} + I_C R_C = 10$$

$$V_{CE} = 10 - 20 \times 200 \times 10^{-3} = 6 \text{ V}$$

Operating point defined by :

I_c = 20 mA and V_{cE} = 6V

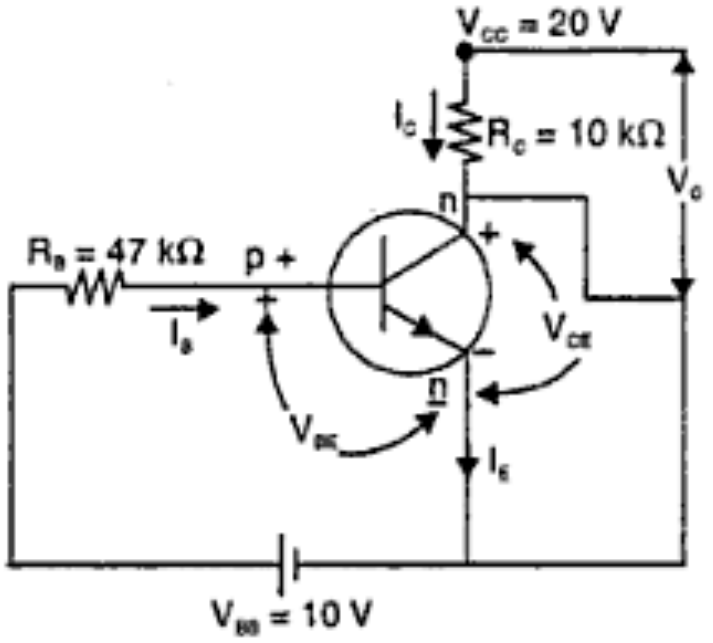


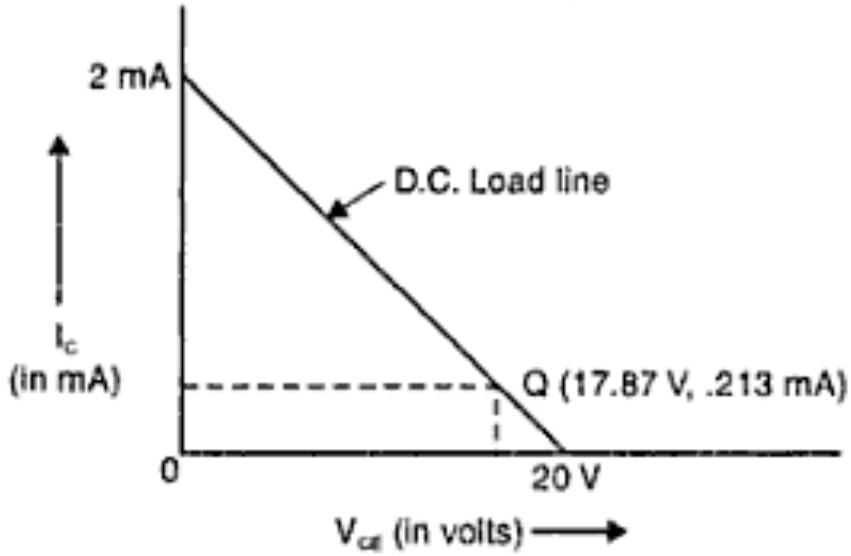
Q: Explain the DC load line analysis of a transistor, Dependency of Q point , temperature , β

DC Load Line

- It is a straight line drawn on the output characteristic of the transistor.
- DC Load Line is used for analyzing the performance of an AMPLIFIER,
- It is a graph of Collector current (Ic) versus Collector Emitter voltage (Vce) for a given value of Rc and Vcc.
- It is a graphical representation of all the possible operating points for the given circuit with the given DC biasing.

How to plot a DC load line?





Step 1. Applying KVL in the output of circuit.

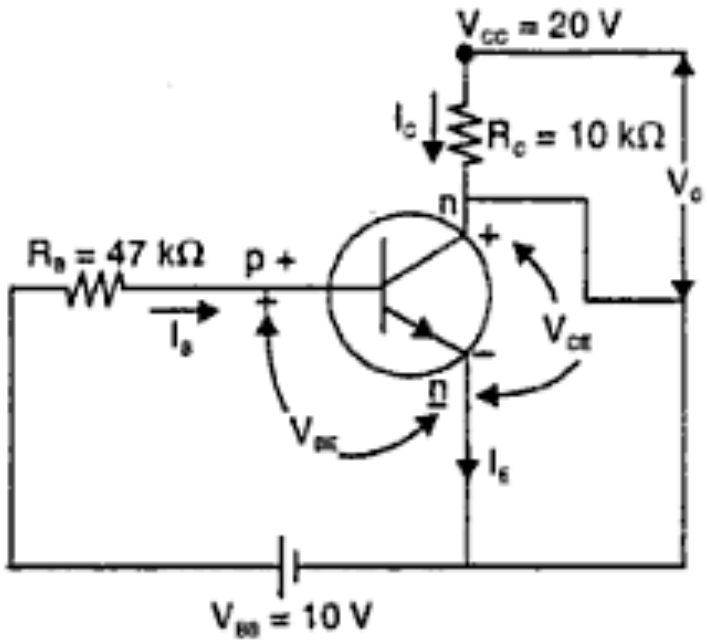
$$V_{CC} - I_C R_C - V_{CE} = 0$$

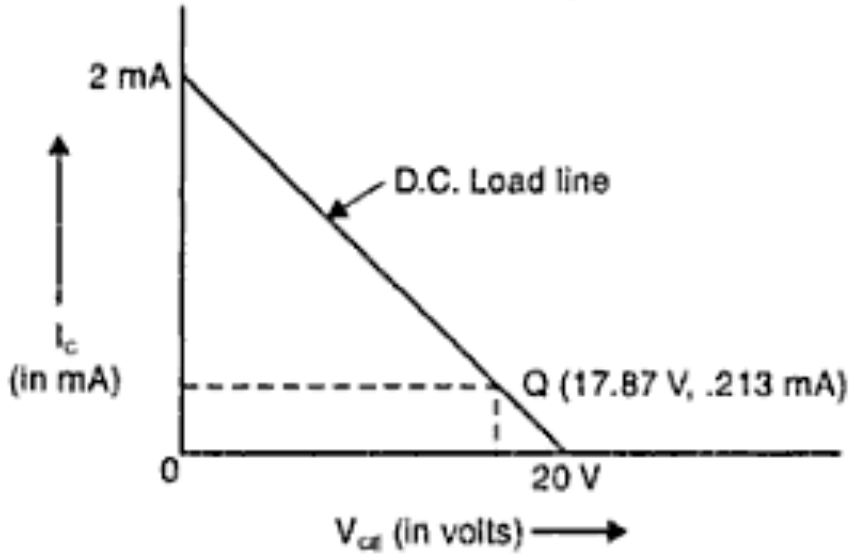
$$V_{CC} = I_C R_C + V_{CE}$$

Step 2. On putting $V_{CE} = 0$, we get

$$I_C = \frac{V_{CC}}{R_C} = \frac{20}{10\ \text{k}\Omega} = 2\ \text{mA}.$$

How to plot a DC load line?





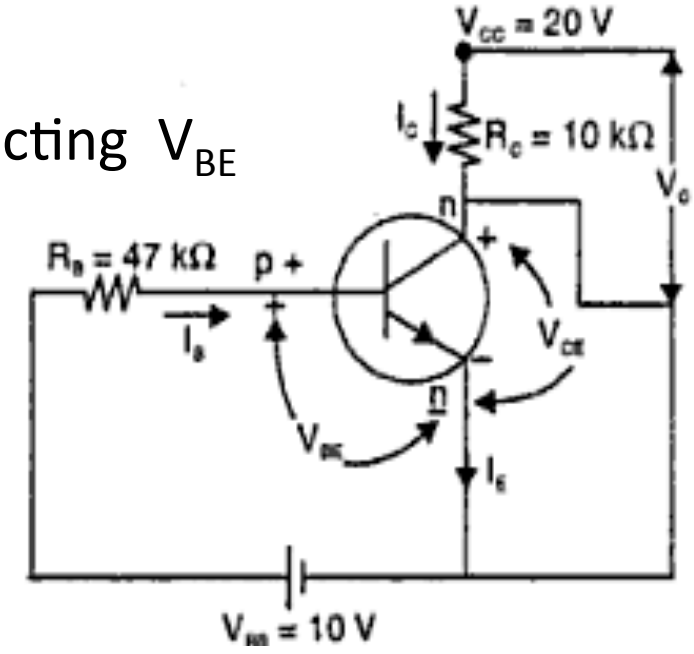
Step 3. On putting $I_C = 0$ in eqn. we get,

$$V_{CE} = V_{CC} = 20 \text{ V}$$

Step 4. Join these values (*i.e.*, $I_C = 2$ mA and $V_{CE} = 20$ V) as shown in Fig.

To find the Q point for previous problem?

Applying KVL to the input section and neglecting V_{BE}



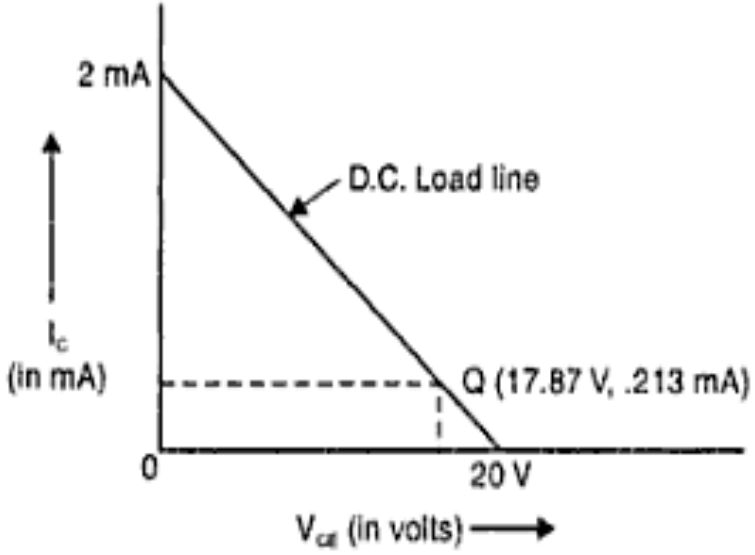
$$V_{BB} = I_B R_B$$

$$I_B = \frac{V_{BB}}{R_B} = \frac{10}{47\ \text{k}\Omega} = .213\ \text{mA}$$

$$I_C = \beta\ I_B = 100 \times .213 = 21.3\ \text{mA}$$

Applying KVL to the output section:

$$V_{CE} = V_{CC} - I_C R_C$$
$$V_{CE} = 20 - .213 \times 10^{-3} \times 10 \times 10^3$$
$$V_{CE} = 17.87\ \text{V}.$$



The quiescent point (17.87 V, .213 mA) is shown in Fig.

Q: Dependency of Q point on temperature and β

STABILIZATION

OPERATING POINT is the zero signal values of (I_c, V_{CE}).

If either of the two changes, the operating point is shifted.

Causes of unstabilization?

- A transistor is said to be unstabilized when its operating point is shifted, due to changes in collector current.

- The Collector current in a transistor changes rapidly due to following reasons:

1. ***Inherent variations of transistor parameters:***

   If the transistor is replaced by another one of the same type.

   (*Because no two transistor can have same transistor parameters (i.e. β)*

2. ***The temperature changes affects Ic***.

How does Temperature change affect Ic.

$$I_c = \beta I_B + I_{CEO}$$

- Leakage current *Ico* increases due to increase in temperature.
- Increase in *Ico* increases *Ic* .
- Rise in *Ic* increases temperature.
- Rise in Temp. further increases *Ic.*
- Rise in *Ic* further increases Temp. , Temp. rise further increases *Ico* , increase in *Ico* futher increases Ic and hence temp and so on.

Cumulative Effect: **THERMAL RUNAWAY**

Self destruction of transistor

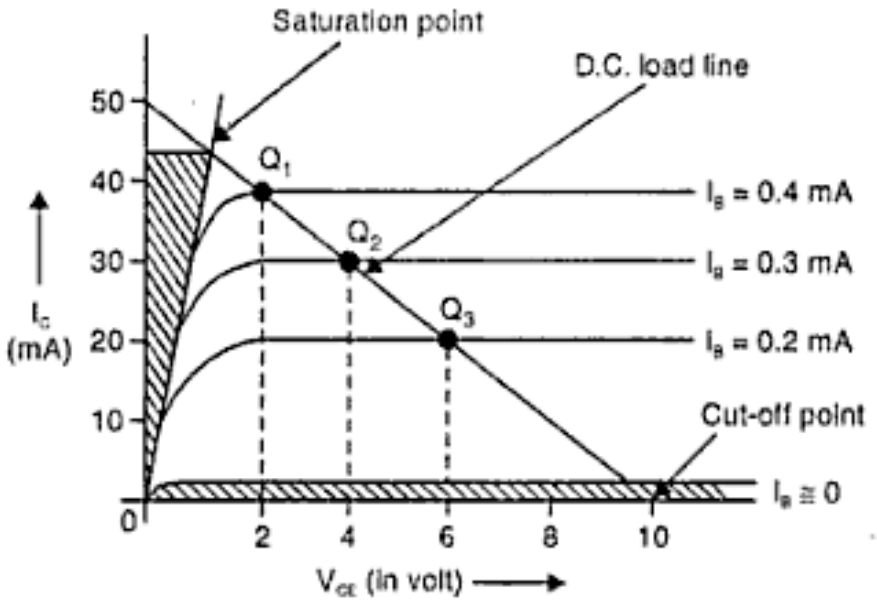
Operation point stabilization

The process of making operating point independent of temperature changes or inherent variation in transistor parameters is called STABILIZATION

TRANSISTOR BIASING

What is transistor DC biasing ?

Biasing is selection of operating point (Quiescent point) to operate a transistor in a desired region (Active, cutoff, saturation)



Biasing Circuit:

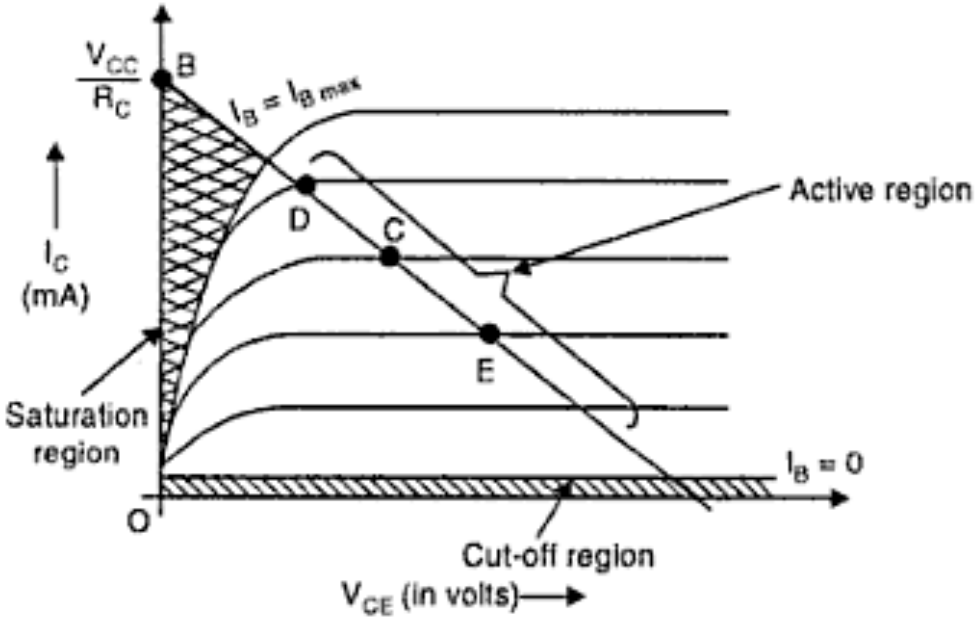
The circuitry which provides the necessary conditions of transistor biasing is known as biasing circuit.

Need of Transistor Biasing

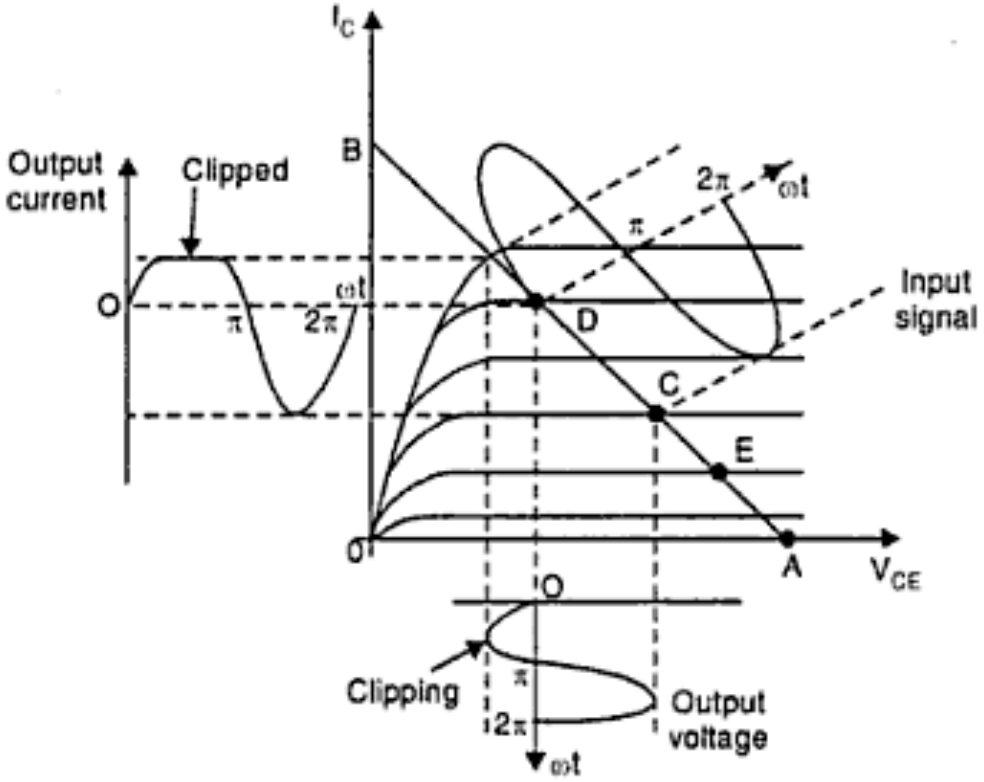
For Transistor as an amplifier:

After applying input AC signal

Operating point should always remain in ACTIVE REGION

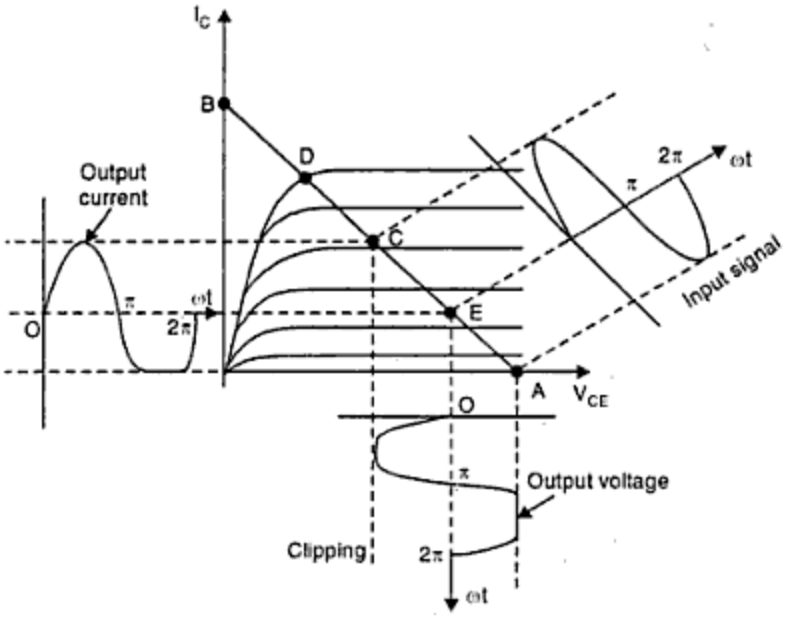


Operating Point in ACTIVE REGION ?



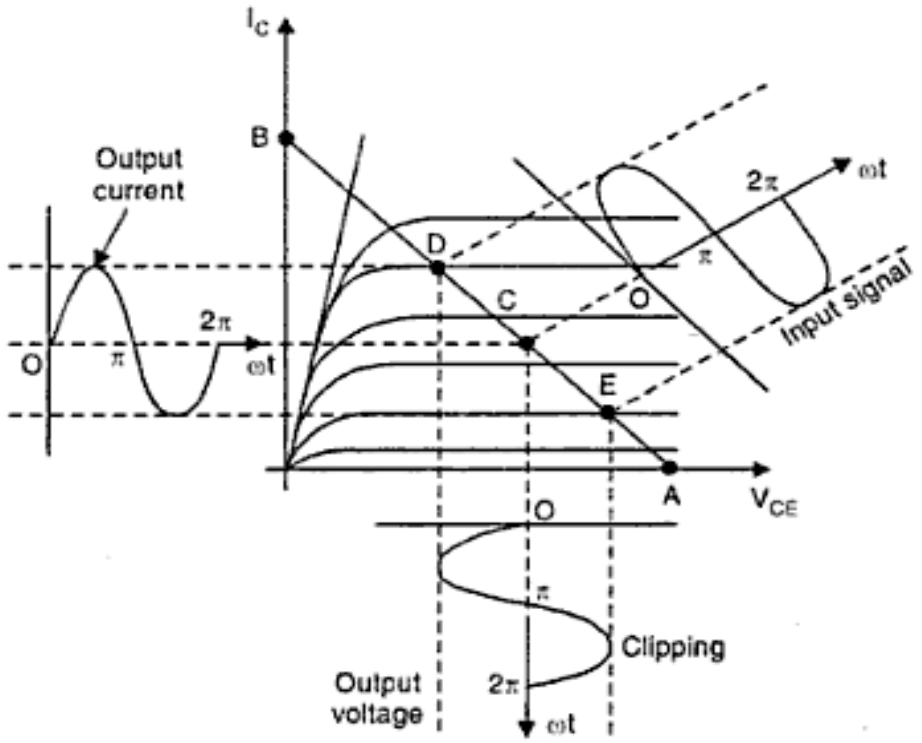
Output characteristics if D is selected as the operating point.

Operating Point in ACTIVE REGION ?



Output characteristics if E is selected as the operating point.

Operating Point in ACTIVE REGION ?



Output characteristics if C is selected as the operating point.

Requirements of Transistor Biasing Circuit ?

1. It should ensure proper zero signal I_c and V_{cE}

   i.e. operating point should be established in the center of the ***active region*** *of the characteristics, so that signal may not cutoff at any part.*

2. It should make the operating point independent of transistor parameters.

   So that it does not shift when the transistor is replaced with another of the same type in the circuit.

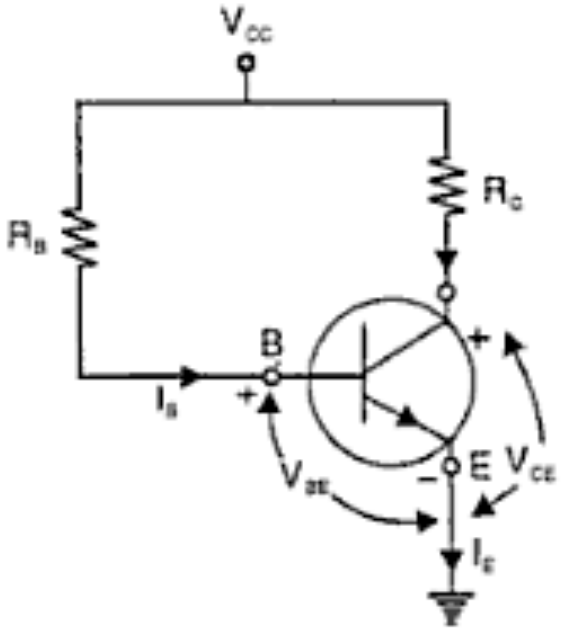
3. Stabilize the collector current against temperature variation.

Different Biasing Circuits

1. Fixed Biasing or Base Resistor Bias.
2. Collector to base Biasing.
3. Emitter resistor biasing
4. Potential divider biasing

Analysis of fixed bias circuit

Operating Point:



Fixed biasing circuit for npn transistor.

To find I_c and V_{CE}

To find I_c ?

Apply KVL to the input side and find I_B

Find I_C by equation: $I_c = \beta I_B$

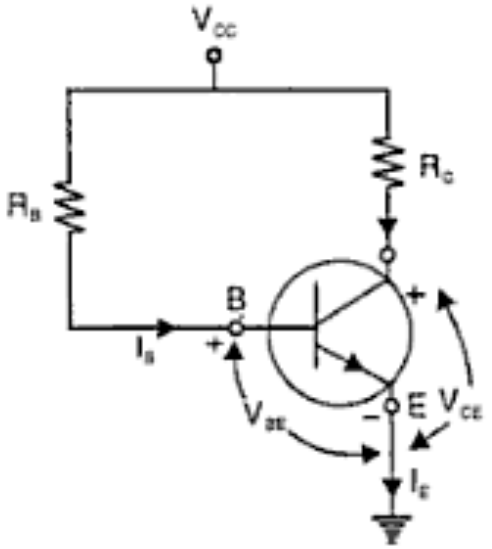
Find V_{CE} by applying KVL to the outer loop

Fixed Bias (Base Resistor Biasing)

1. In this biasing a high valued resistor is connected between the supply and base of the transistor.

2. The Base emitter junction is forward biased and the base collector junction is reverse biased by the supply voltage Vcc.

3. For a pnp transistor the negative end of the supply is to be connected to the Rc and Rb.



Fixed biasing circuit for npn transistor.

Q : Draw and Explain Base resistor method of biasing

Q : Draw and Explain Base resistor method of biasing

To calculate I_c :

Apply KVL to the input section

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$I_c = \beta I_B + I_{CEO}$$

Neglecting , I_{CEO}

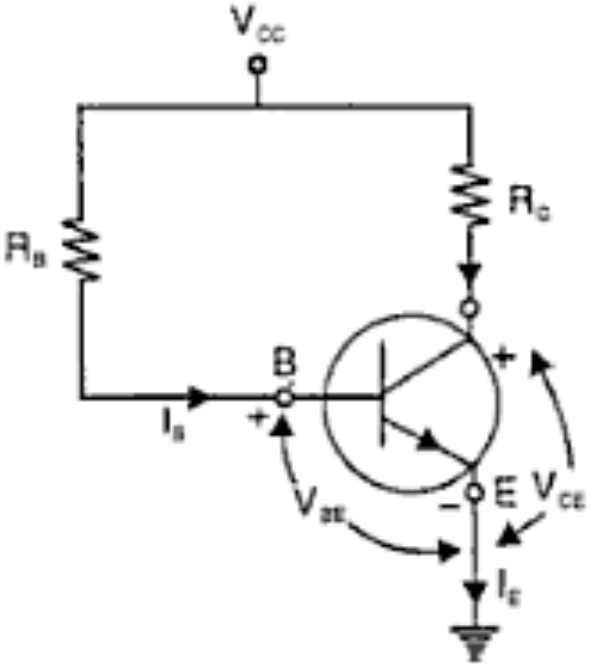
$$I_c = \beta I_B$$

To calculate V_{cE} :

Apply KVL to outer loop:

$$V_{cc} = I_c R_c + V_{cE}$$

$$V_{cE} = V_{cE} - I_c R_c$$



Fixed biasing circuit for npn transistor.

Operating point : (I_c , V_{CE})

Advantages of Fixed Bias:

- Calculations are simple
- Simple in construction

  Only two resistors and a battery is needed
- Easy to fix the operation point anywhere in the active region of the characteristic.

  By simply changing the value of Rb.

Q : Draw and Explain Base resistor method of biasing

Disadvantages of Fixed Bias:

- Operating point can be fixed in the center of the active region.

But it miserably fails in the other two requirements of the biasing circuit.

- Operating point is not stable w.r.t temperature rise and transistor parameter β

Q : Draw and Explain Base resistor method of biasing

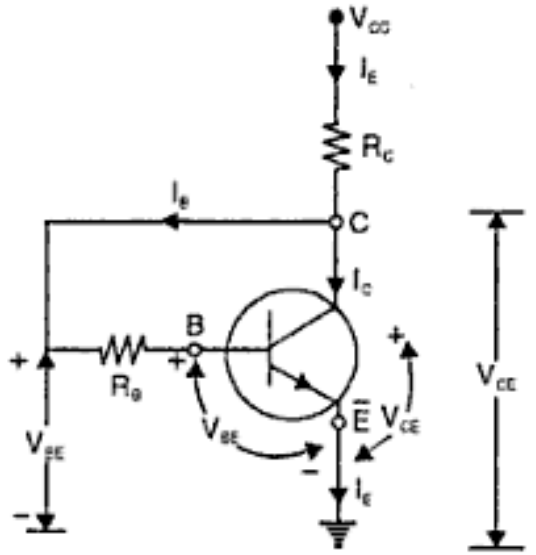
Collector to Base Biasing

1. In this biasing a very high value resistance Rb is connected between the collector and base, and Rc is connected between Supply voltage and collector of transistor .
2. The base current Ib feedbacks from the output.

The base current I_b depends upon the collector voltage.

This circuit is also called as

VOLTAGE FEEDBACK BIASING CIRCUIT.



Collector-to-base biasing for an npn transistor.

Analysis of Collector to base bias

To calculate I_c :

Apply KVL to inner loop:

$$V_{CC} - (I_B + I_C) R_C - I_B R_B - V_{BE} = 0$$

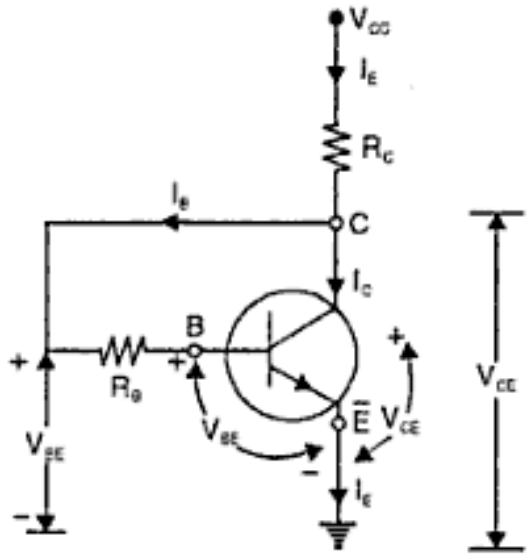
$$I_c = \beta I_b$$

$$\therefore \quad V_{CC} - V_{BE} = (I_B + \beta I_B) R_C + I_B R_B$$

$$\therefore \quad V_{CC} - V_{BE} = I_B [(1 + \beta) R_C + R_B]$$

$$\therefore \quad \boxed{I_B = \frac{V_{CC} - V_{BE}}{(1 + \beta) R_C + R_B}}$$

$$I_c = \beta I_b$$



Collector-to-base biasing for an npn transistor.

Collector to Base Biasing

To calculate V_{cE} :

Apply KVL to outer loop:

$$V_{cc} = (I_c + I_B) R_c + V_{cE}$$

$$\boxed{V_{CE} = V_{CC} - (I_B + I_C) R_C}$$

Advantages of collector to base bias

Tendency of the circuit to stabilize the operating point against temperature variations and transistor parameter variations

Advantages of collector to base bias

- If there is an increase in β due to piece variation. OR
- If there is a increase in β and Ico due to the change in temperature.

$I_c = \beta I_B + I_{CEO}$ Ic increases

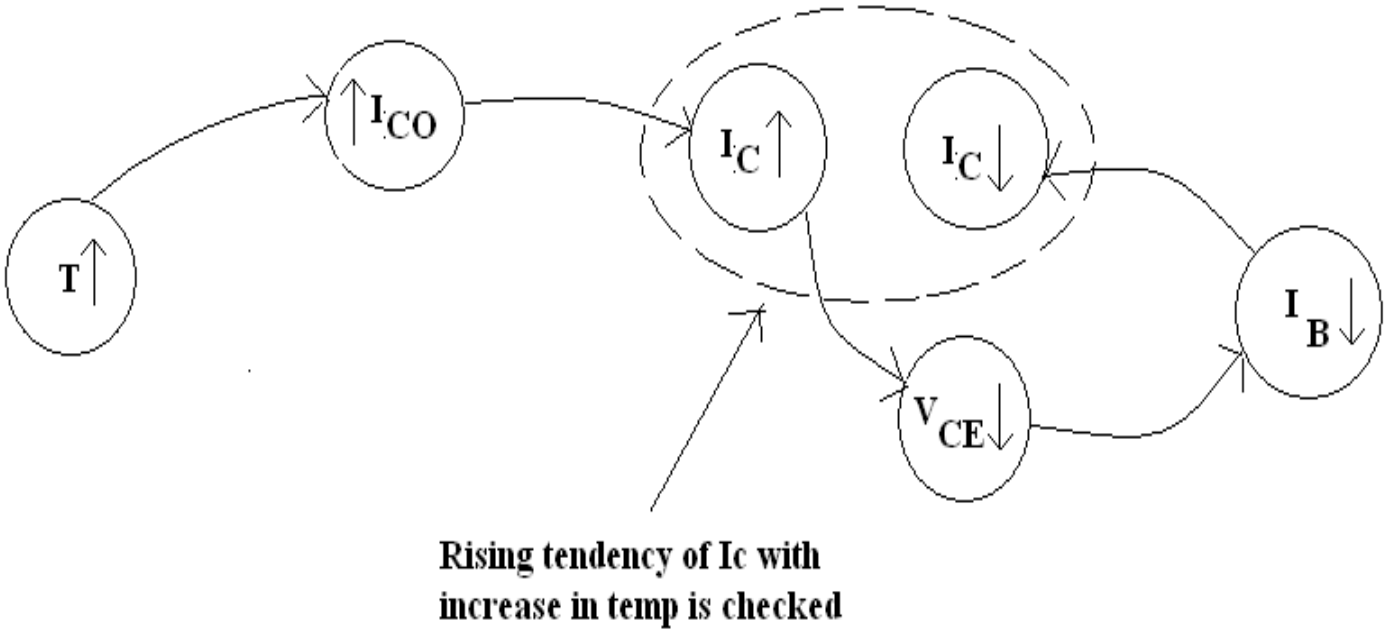
$V_{cE} = V_{cc} - I_c R_c$ V_{cE} decreases

$I_B = \frac{V_{CE} - V_{BE}}{R_C + R_B}$ I_B decreases

$I_c = \beta I_b$ I_c decreases

Rising tendency in I_c is checked

Advantages of collector to base bias



Advantages of collector to base bias

- I_c depends on I_b.
- Decrease in I_b reduces the original increase in I_c (Negative feedback).
- Therefore the circuit maintains a stable value of collector current, keeping Q point fixed.

Collector to Base bias is seldom used ?

- The resistor R_B also provides ac feedback.

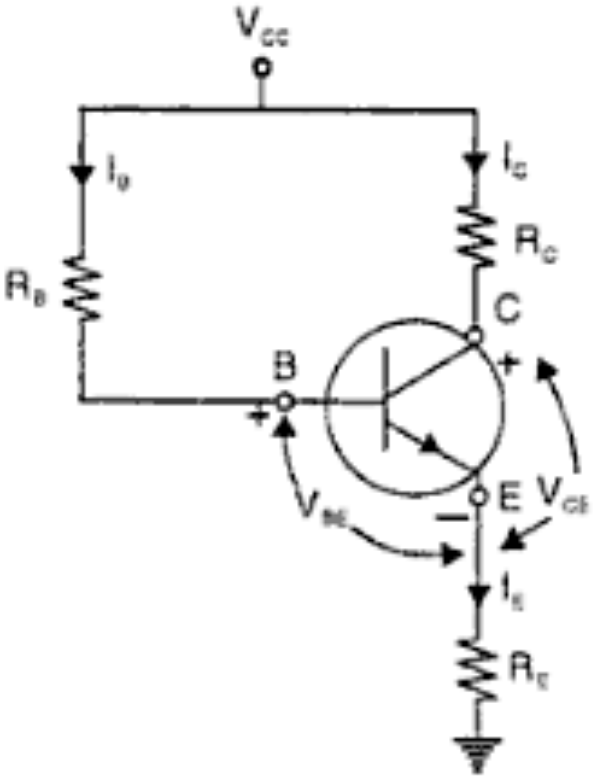
This reduces the voltage gain of the amplifier.

Emitter Resistor Biasing

- It is just a modification to the Base Resistor Biasing circuit.

- In this biasing an additional resistor R_E is connected in the emitter.

- Hence, this circuit contains three resistors R_B, R_C and R_E.



Emitter biasing circuit for an npn transistor.

Analysis of operating point

Writing the loop equation for input circuit, we get

$$V_{CC} = I_B R_B + V_{BE} + I_E R_E$$

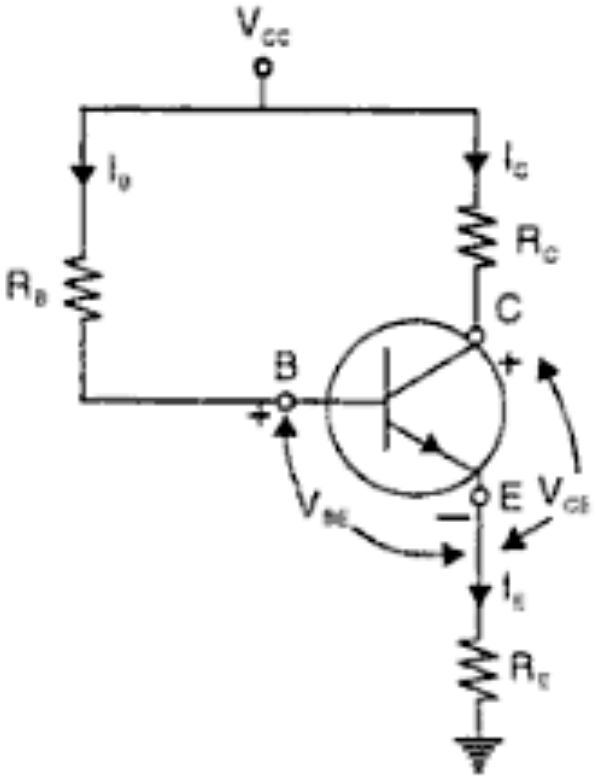
$$V_{CC} = I_B R_B + V_{BE} + (\beta+1) I_B R_E \qquad (\text{since } I_E = (\beta+1) I_B)$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta+1) R_E}$$

Neglecting V_{BE} since it is very small

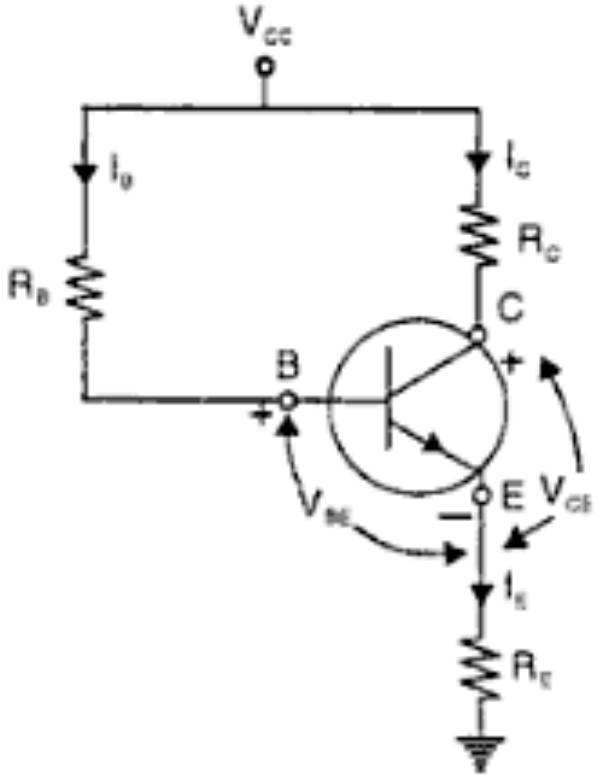
$$I_B \approx \frac{V_{CC}}{R_B + \beta R_E}$$

Collector current, $I_C = \beta I_B = \dfrac{\beta V_{CC}}{R_B + \beta R_E} = \dfrac{V_{CC}}{R_E + (R_B / \beta)}$



Emitter biasing circuit for an npn transistor.

Analysis of operating point



Emitter biasing circuit for an npn transistor.

Writing the loop equation for the output circuit, we get

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$V_{CE} = V_{CC} - (R_C + R_E) I_C \qquad (I_C \approx I_E)$$

Thus, operating point can be obtained from above equations.

Similarly, for the given operating point, the value of R_B and R_E can be determined from the above equations provided the other data via V_{CC}, R_C and β are known.

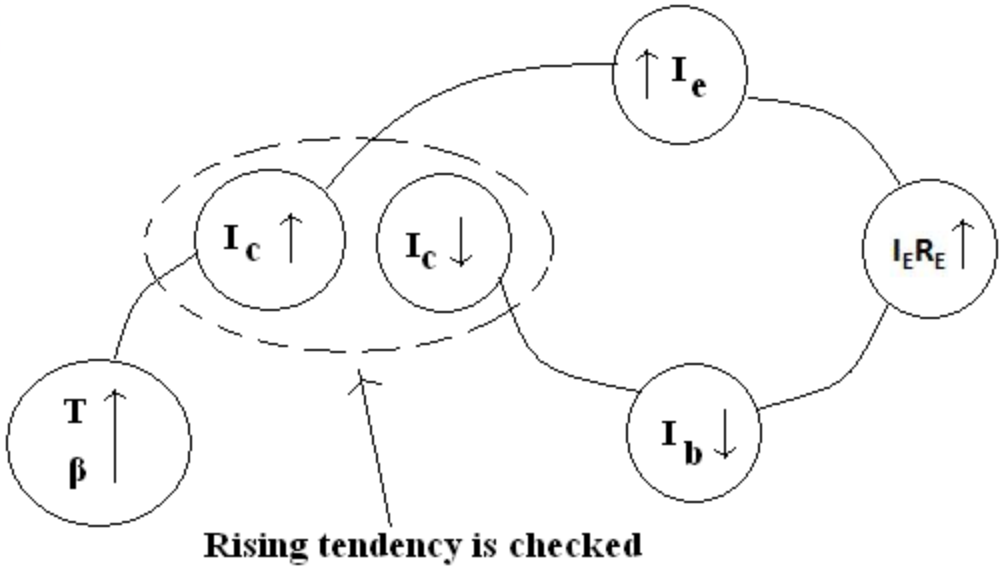
Stabilization

$$V_{CC} = I_B R_B + V_{BE} + I_E R_E$$

$$I_B = \frac{V_{CC} - I_E R_E - V_{BE}}{R_B}$$

(since V_{BE} is very small)

$$I_B \approx \frac{V_{CC} - I_E R_E}{R_B}$$



•Thus, an increase in collector current is brought back to its previous value by the sequence of events.

•Hence, the stablility of the operating point is improved to large extent by inserting a resistor in emitter circuit.

Advantages

- The stability factor of this biasing is quite high.
- Hence, the operating point does change, although to lower extent, due to temperature rise or inherent variations in parameters.
- The **DC feedback** helps in the stabilization of operating point .
- But at the same time **AC feedback** reduces the voltage gain of the amplifier.
- This is an undesirable feature.
- However, this drawback can be remedied by **putting a capacitor C_E across the resistor R_E**. The capacitor C_E offers very low impedance to the AC current and does not allow it to pass through R_E and hence AC feedback is restricted. Thus, the process of amplification remains unaffected

Drawback of Emitter bias

This biasing circuit is also **not practically used** because of the following reason:

$$I_c = \beta I_b$$

$$\text{i.e. } I_C = \frac{V_{CC}}{R_E + (R_B/\beta)}$$

For stability, Ic should be independent of β

i.e denominator should be independent of β

$$R_E >> R_B/\beta$$

$$\text{i.e. } I_C = \frac{V_{CC}}{R_E + (R_B/\beta)} \qquad R_E >> R_B/\beta$$

- This condition can only be obtained either using R_E of very large value or by using R_B of very small value.

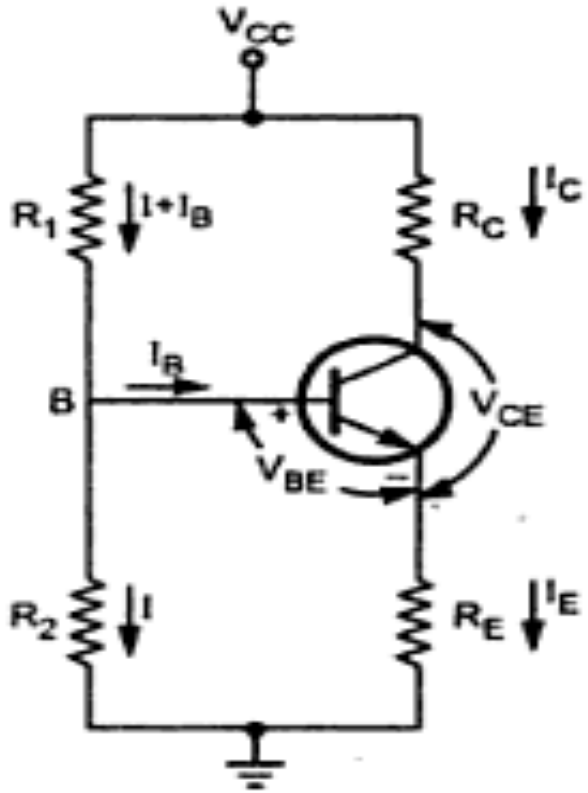
- Now, a large value of R_E will cause a large voltage drop across it and to obtain a required operating point, we have to apply a voltage source V_{CC} of high value.

- On the other hand, if R_B is of very low value , a separate low voltage supply has to be used for base circuit.

- ***Both these alternatives are quite impractical. Hence, this biasing circuit is not used practically.***

Voltage Divider Bias

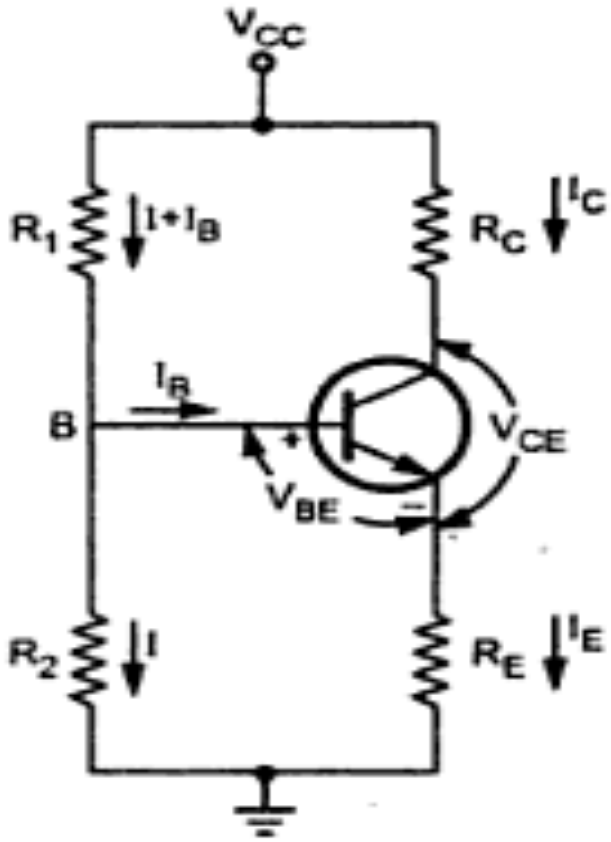
- Most widely used biasing circuit.



Voltage divider bias circuit

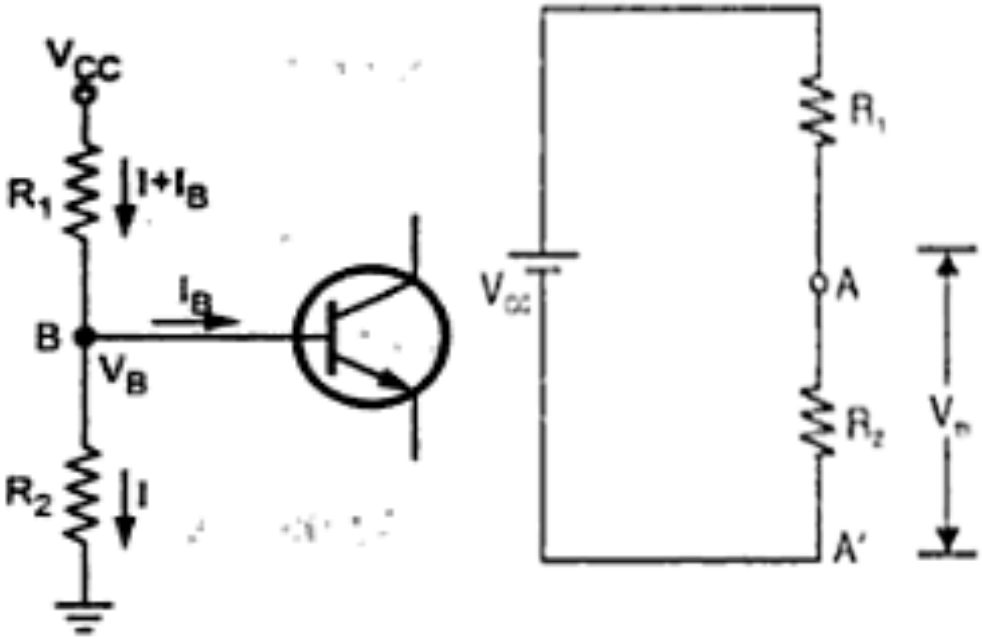
Q : Draw and Explain Voltage Divider method of biasing

Analysis of Operating Point: (I_c and V_{CE})



Voltage divider bias circuit

Input Circuit



Base circuit

V_B can be given by

$$V_B = \frac{V_{CC} \times R_2}{R_1 + R_2}$$

Voltage Divider Bias

Output Circuit

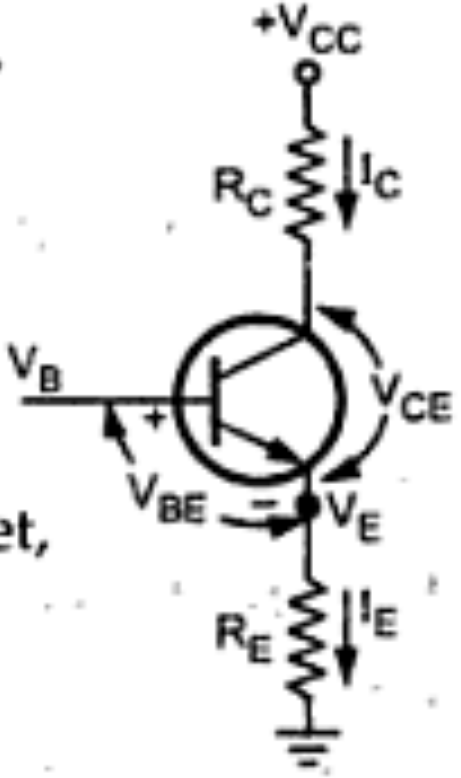
Now, let us consider the collector circuit

Voltage across R_E (V_E) can be obtained as,

$$V_E = I_E R_E = V_B - V_{BE}$$

$$\therefore \quad I_E = \frac{V_B - V_{BE}}{R_E}$$

$$I_C \approx I_E$$



Applying KVL to the collector circuit we get,

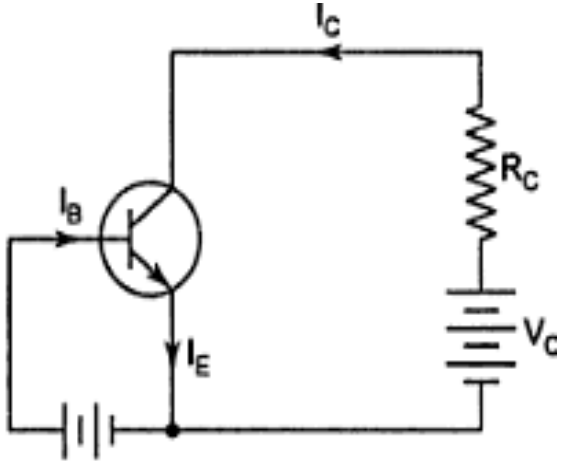
$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

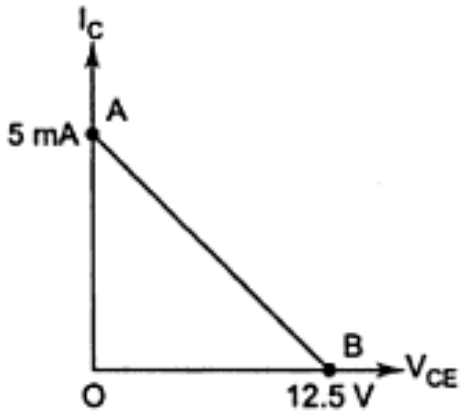
$$\therefore \quad V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

Operating point : (I_c , V_{CE})

Problems

1. For the circuit shown plot the DC load line





The collector-emitter voltage V_{CE} is given by :

$$V_{CE} = V_{CC} - I_C R_C$$

$$I_C = 0$$

$$V_{CE} = V_{CC} = 12.5 \text{ V}$$

This locates the point B of the load line on the collector-emitter voltage axis.

When $V_{CE} = 0$

$$I_C = \frac{V_{CC}}{R_C} = \frac{12.5 \text{ V}}{2.5 \text{ k}\Omega} = 5 \text{ mA}$$

This locates the point A of the load line on the collector current axis. By joining these two points, we get the d.c. load line AB

2. *In a transistor circuit, collector load is 4 kΩ whereas quiescent current (zero signal collector current) is 1 mA.*

(i) What is the operating point if $V_{CC} = 10$ V ?

(ii) What will be the operating point if $R_C = 5$ kΩ ?

$V_{CC} = 10$ V, $I_C = 1$ mA

(*i*) When collector load,

$$R_C = 4 \text{ k}\Omega$$

$$V_{CE} = V_{CC} - I_C R_C = 10 - 1 \text{ mA} \times 4 \text{ k}\Omega = 10 - 4 = 6 \text{ V}$$

$\therefore$ Operating point is **6 V, 1 mA.**

(*ii*) When collector load,

$$R_C = 5 \text{ k}\Omega$$

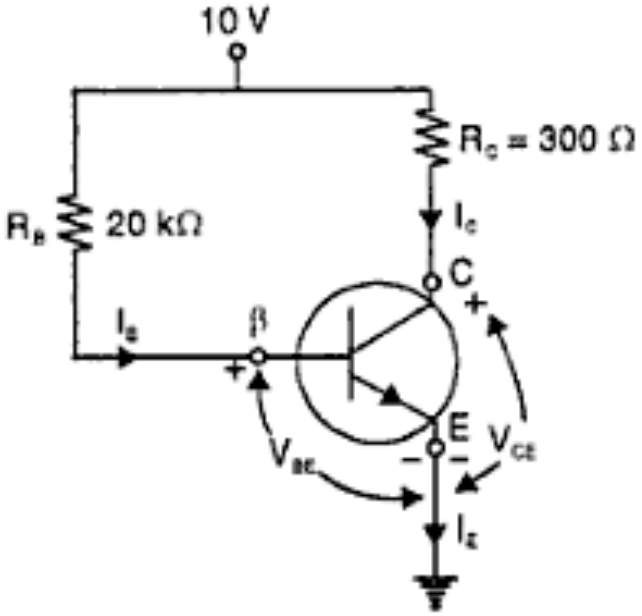
$$V_{CE} = V_{CC} - I_C R_C = 10 - 1 \text{ mA} \times 5 \text{ k}\Omega = 10 - 5 = 5 \text{ V}$$

$\therefore$ Operating point is **5 V, 1 mA.**

3. *A base resistor biasing circuit is shown in Fig. Determine (assume V_{BE} = 0.6 V and β = 60).*

(i) *The collector current I_C.*

(ii) *Collector emitter voltage V_{CE}*



Given

V_{BE} = 0.6 V

V_{CC} = 10 V

β = 60

R_B = 20 kΩ

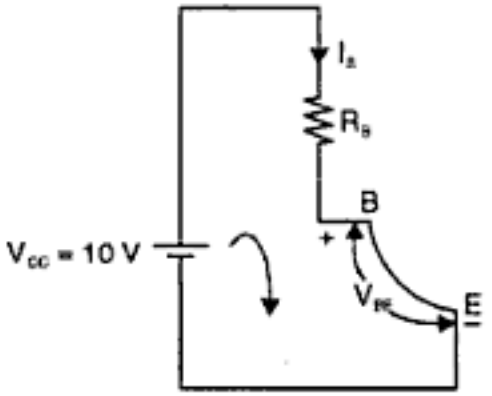
R_C = 300 Ω

Applying KVL in the input section.

$$10 - I_B R_B - V_{BE} = 0.$$

$$I_B = \frac{10 - V_{BE}}{R_B} = \frac{10 - .6}{20\ k\Omega} = \frac{9.4\ V}{20\ k\Omega} = .47\ mA.$$

$$I_C = \beta\ I_B = 60 \times .47 = 28.2\ mA.\ \textbf{Ans.}$$



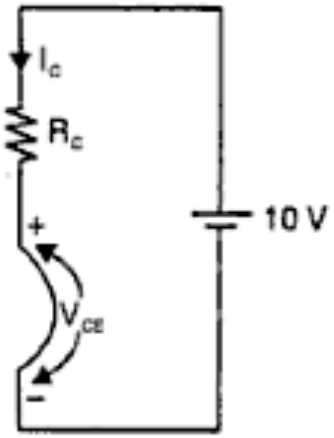
(*ii*) Again, applying the KVL in the output section

$$10 - I_C R_C - V_{CE} = 0.$$

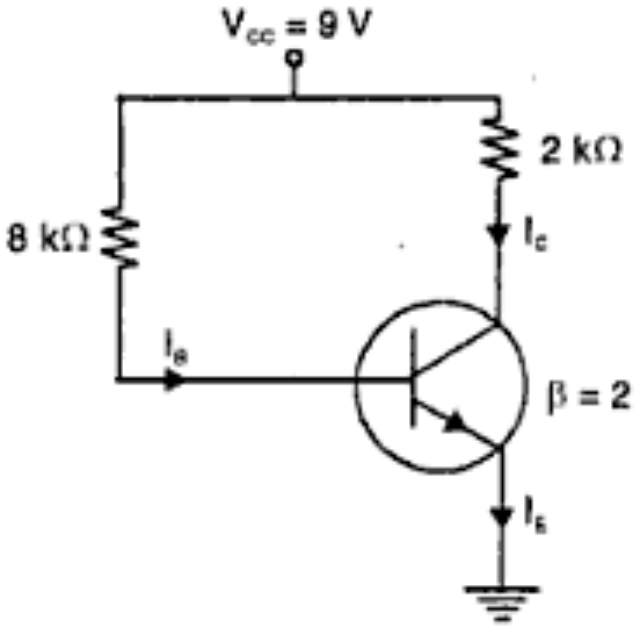
$$V_{CE} = 10 - I_C R_C$$

$$= 10 - 28.2 \times 300 \times 10^{-3}$$

$$V_{CE} = 1.54 \text{ V.} \quad \textbf{Ans.}$$



4. *Draw the dc load line and locate the operating point for the fixed biasing transistor circuit shown in (assume V_{BE} = .6 V)*



DC Load Line

Applying KVL to the output the circuit.

$$V_{CC} - I_C R_C - V_{CE} = 0$$

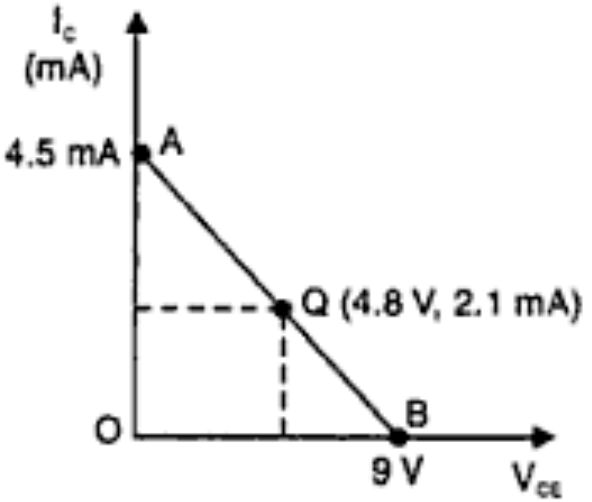
On putting the value V_{CE} = 0 in eqn. (1), we get

$$I_C = \frac{V_{CC}}{R_C} = \frac{9}{2\ \text{k}\Omega} = 4.5\ \text{mA (assume OA)}$$

On putting the value of I_C = 0. In eqn. (1), we get,

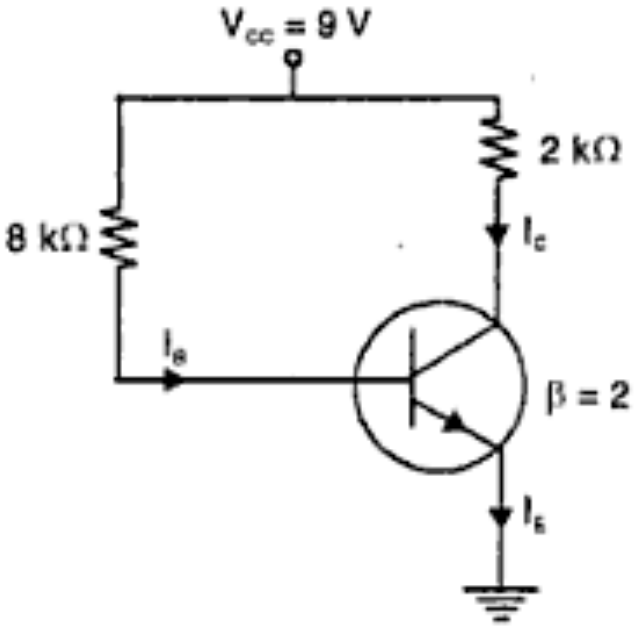
$$V_{CE} = V_{CC} = 9\ \text{V (assume OB)}$$

To draw the load line join the values OA and OB.



4.

Operating Point



Now, $I_B = \dfrac{V_{CC} - V_{BE}}{R_B} = \dfrac{9 - .6}{8\ \text{k}\Omega} = \dfrac{8.4}{8} = 1.05\ \text{mA}$

$$V_{CE} = V_{CC} - I_C R_C$$

$$= 9 - \beta\, I_B R_C$$

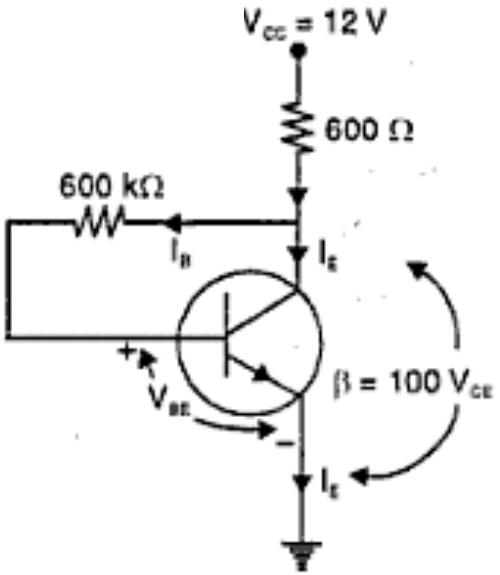
$$= 9 - 2 \times 1.05 \times 2 = 9 - 4.2 = 4.8\ \text{V}$$

$$I_C = \beta\, I_B = 2 \times 1.05 = 2.1\ \text{mA}$$

Hence, operating point $Q\ (V_{CE}, I_C) = 4.8\ \text{V}, 2.1\ \text{mA}$.

5.

For the circuit determine the emitter current the collector voltage V_C. Neglecting V_{BE}.



Since emitter is grounded so

$$\left.\begin{aligned} V_{CE} = V_C \quad \therefore \quad V_{CE} &= V_C - V_E \\ &= V_C - 0 \\ &= V_C \end{aligned}\right\}$$

Now applying KVL to the input side

$$V_{CC} - I_E\,(600) - I_B \times 600 \times 10^3 - V_{BE} = 0$$

$$V_{CC} - (I_B + I_C)\,600 - I_B \times 600 \times 10^3 = 0 \quad \{\because\ V_{BE} = 0\}$$

$$V_{CC} - (I_B + I_B \cdot \beta)\,600 - I_B \times 600 \times 10^3 = 0$$

$$I_B = \frac{V_{CC}}{600 \times 10^3 + 100 \times 600}$$

$$= \frac{12}{600 \times 10^3 + 100 \times 600} = 18.18\ \mu A$$

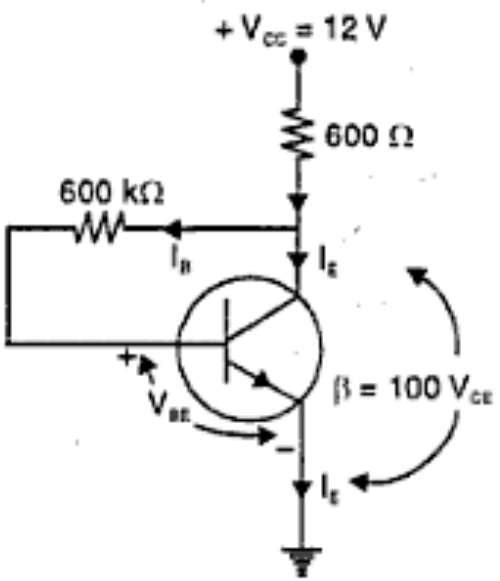
5.

Now, applying KVL to the output circuit.

$$V_{CE} = V_C = V_{CC} - I_C R_C = 12 - 1.818 \times 10^{-3} \times 600$$
$$= 10.91 \text{ V.}$$

$$I_C = \beta I_B = 100 \times 18.18 \text{ mA} = 1.818 \text{ mA.}$$

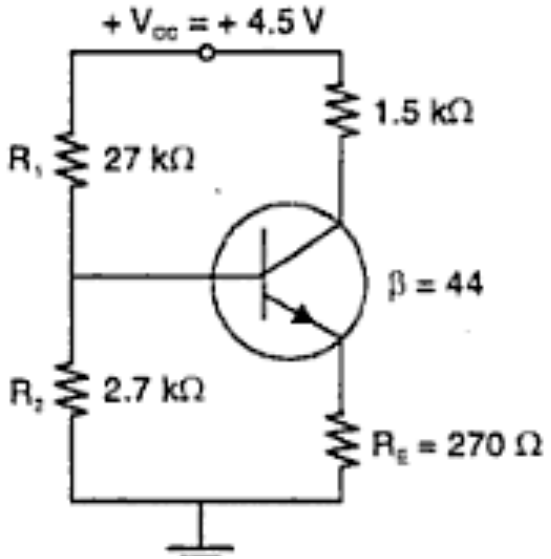
$$I_E = I_C + I_B = 1.818 \text{ mA} + 18.18 \text{ μA} \cong 1.818 \text{ mA.}$$



6. *For the circuit given in Fig. is used in self-biasing arrangement with $\beta = 44$, $R_L = 1.51\ k\Omega$, $R_E = 270\ k\Omega$, and $V_{CC} = 4.5\ V$. (Assume $V_{BE} = 0$) Estimate*

(a) quiescent point

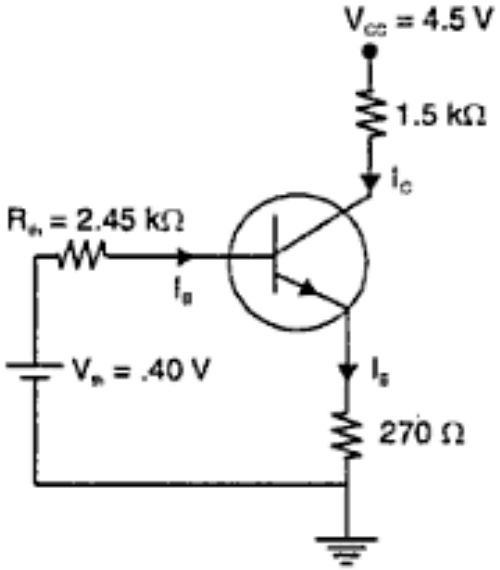
(b) Stability factor.



(a) First we will take the Thevenin equivalent model.

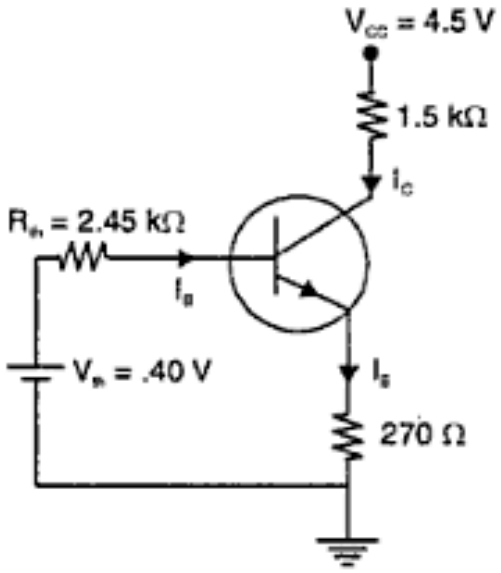
$$V_{th} = 4.5 \times \frac{2.7}{2.7 + 27} = .40\ V$$

$$R_{th} = \frac{R_1 R_2}{R_1 + R_2} = \frac{27 \times (2.7)}{27 + 27} = 2.45\ k\Omega$$



6.

Now applying KVL to the input circuit,



$$V_{th} - I_B R_{th} - V_{BE} - I_E R_E = 0$$

$$V_{th} - I_B R_{th} - V_{BE} - (I_B + I_C) R_E = 0$$

$$V_{th} - I_B R_{th} - V_{BE} - (I_B + \beta I_B) R_E = 0 \quad (\because I_C = \beta I_B)$$

$$I_B = \frac{V_{th} \cdot \beta}{R_{th} + \beta R_E} \quad (\because V_{BE} = 0)$$

$$I_C = \beta I_B = \frac{44\ (.40)}{2.45\ \text{k}\Omega + 44 \times .270\ \text{k}\Omega}$$

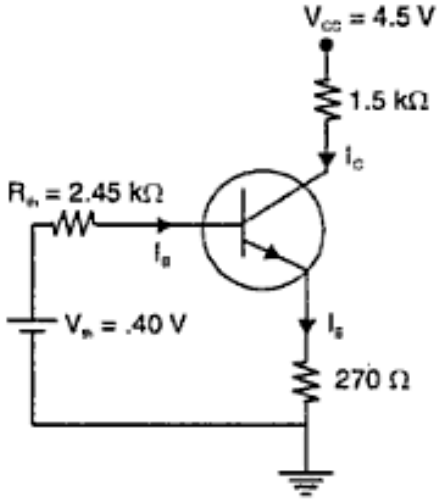
$$I_C = 1.228\ \text{mA}$$

6.

And, applying KVL to the output section,

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$
$$= 4.5 - 1.228\ (1.5 + .270)$$
$$= 4.5 - 2.173 = 2.326\ \text{V}$$



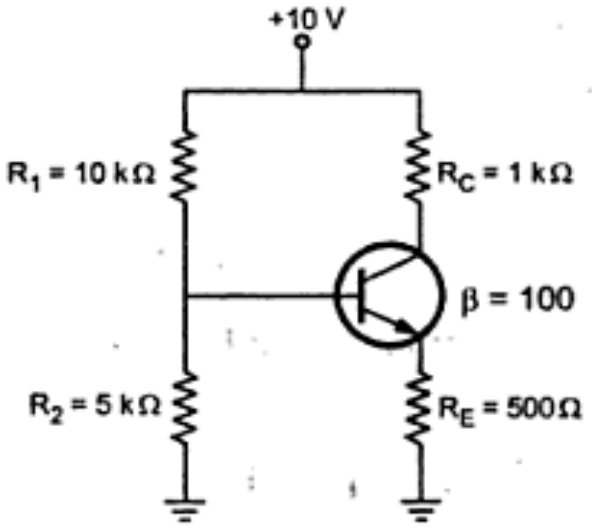
Quiscent Point = (1.228mA, 2.326V)

Stability factor for potential divider biasing

$$S = (\beta + 1)\left[\frac{1 + \frac{R_{th}}{R_E}}{1 + \beta + \frac{R_{th}}{R_E}}\right] = (44 + 1)\left[\frac{1 + \frac{2.45}{.27}}{1 + 44 + \frac{2.45}{.27}}\right]$$

$$= 45\left[\frac{1 + 9.07}{1 + 44 + 9.07}\right] = 8.38 \quad \textbf{Ans.}$$

7. *For the circuit shown in Fig. β = 100 for the silicon transistor. Calculate V_{CE} and I_C.*



$$V_B \cong \frac{R_2}{R_1 + R_2} V_{CC}$$

$$= \frac{5 \times 10^3}{10 \times 10^3 + 5 \times 10^3} \times 10 = 3.33 \text{ V}$$

$$V_E = V_B - V_{BE} = 3.33 - 0.7 = 2.63 \text{ V}$$

$$I_E = \frac{V_E}{R_E} = \frac{2.63 \text{V}}{500} = 5.26 \text{ mA}$$

$$I_B = \frac{I_E}{1 + \beta} = \frac{5.26 \times 10^{-3}}{101} = 52.08 \, \mu\text{A}$$

$$I_C = \beta I_B = 100 \times 52.08 \times 10^{-6} = 5.208 \text{ mA}$$

7.

Applying KVL to the collector circuit we get,

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$= 10 - 5.208 \times 10^{-3} \times 1 \times 10^{3} - 5.26 \times 10^{-3} \times 500 = \mathbf{2.162V}$$