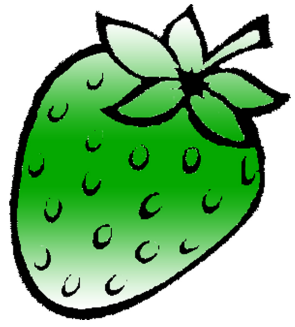
STRAWBERRY



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TIMING DIAGRAMS

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MACHINE CYCLE or BUS CYCLE or INSTRUCTION CYCLE

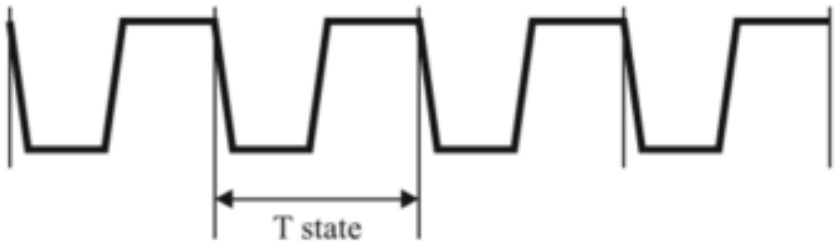
Definition: one discrete information transfer on bus
Also defined as time taken by processor to execute an instruction

Typically, all processor utilizes the following 5 stage cycles:

- Fetch instruction from main memory
- Decode the instruction
- Fetch data from main memory
- Execute Instruction
- Store result

MACHINE CYCLE or BUS CYCLE or INSTRUCTION CYCLE

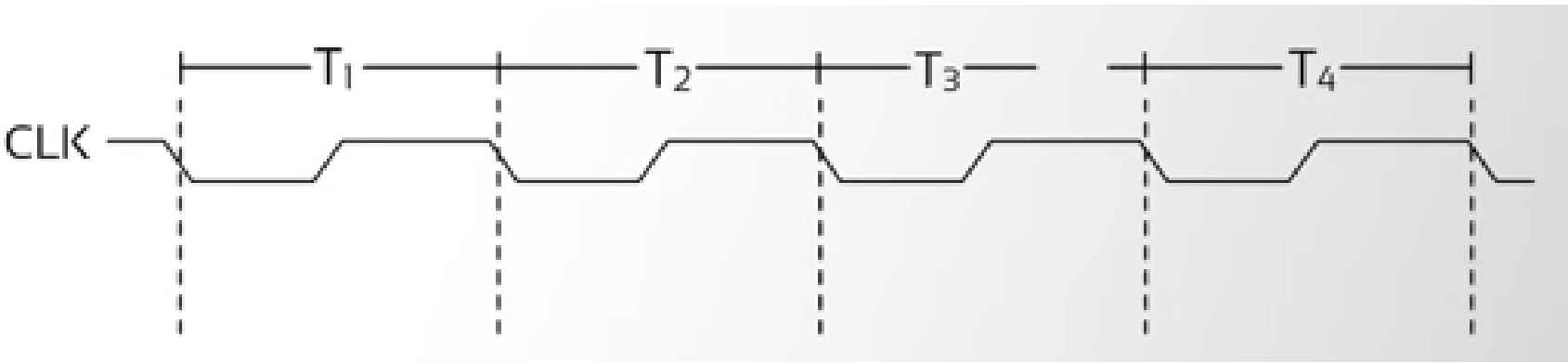
- All these operations are performed w.r.t. CLOCK
- Microprocessor performs an operation in a specific time period i.e. specific clock cycles known as **T-state**
- T-state is time period of a single cycle of the clock frequency



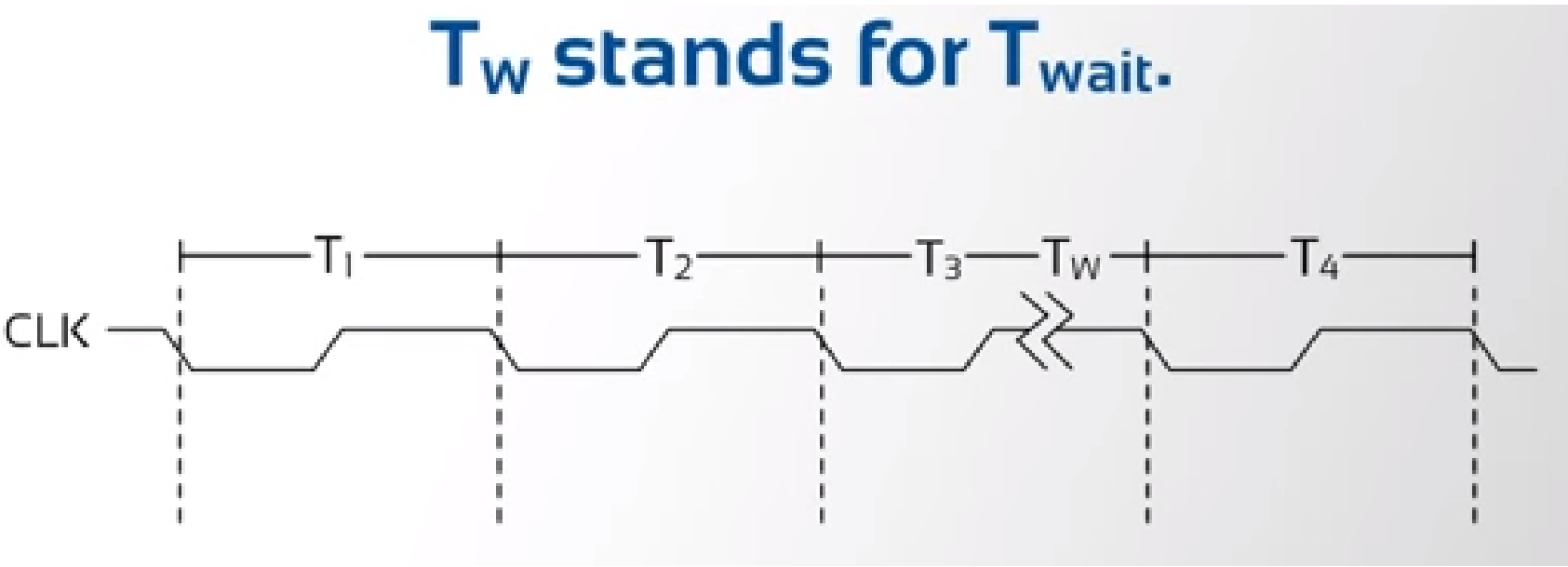
MACHINE CYCLE

- No. of T-state required to access a peripheral is called MACHINE CYCLE
- Access a peripheral means to perform a read or a write operation either from memory or an I/O In 8086 Memory read or memory write require 4 T-states.

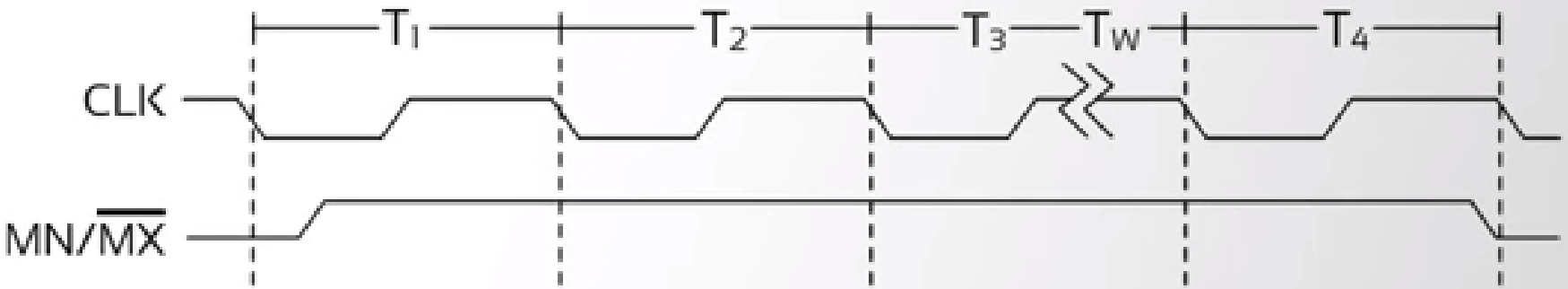
Timing Diagram for a read cycle



Timing Diagram for a read cycle

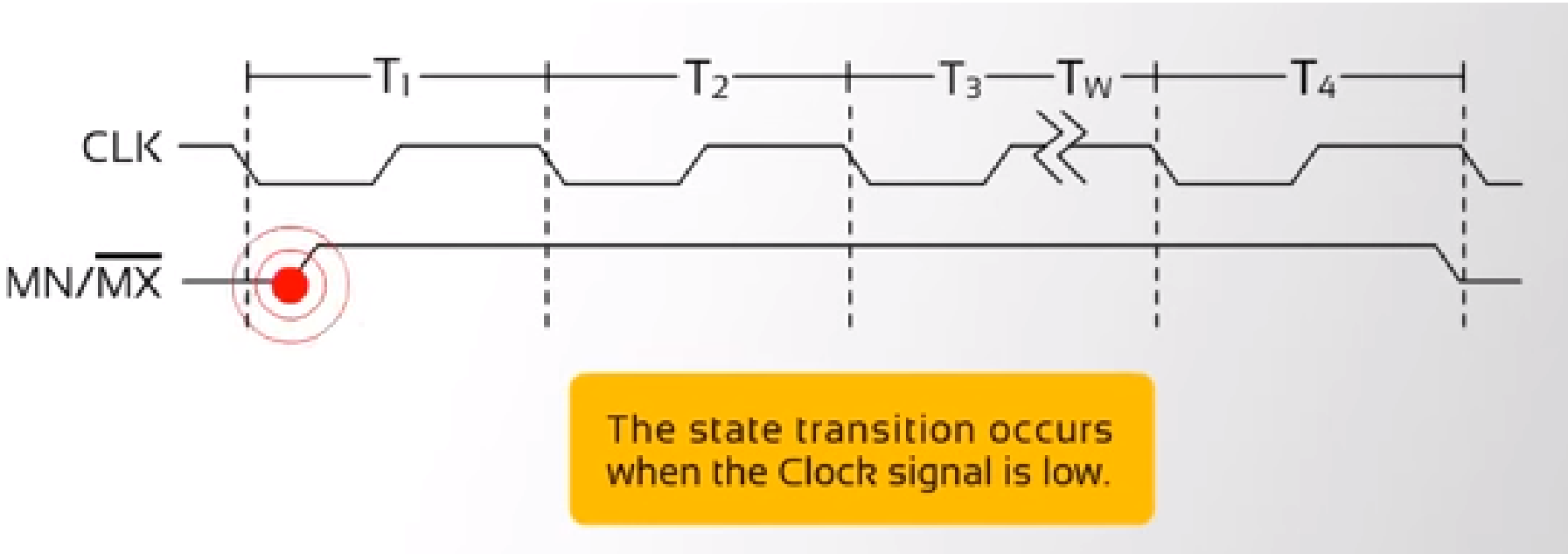


Timing Diagram for a read cycle



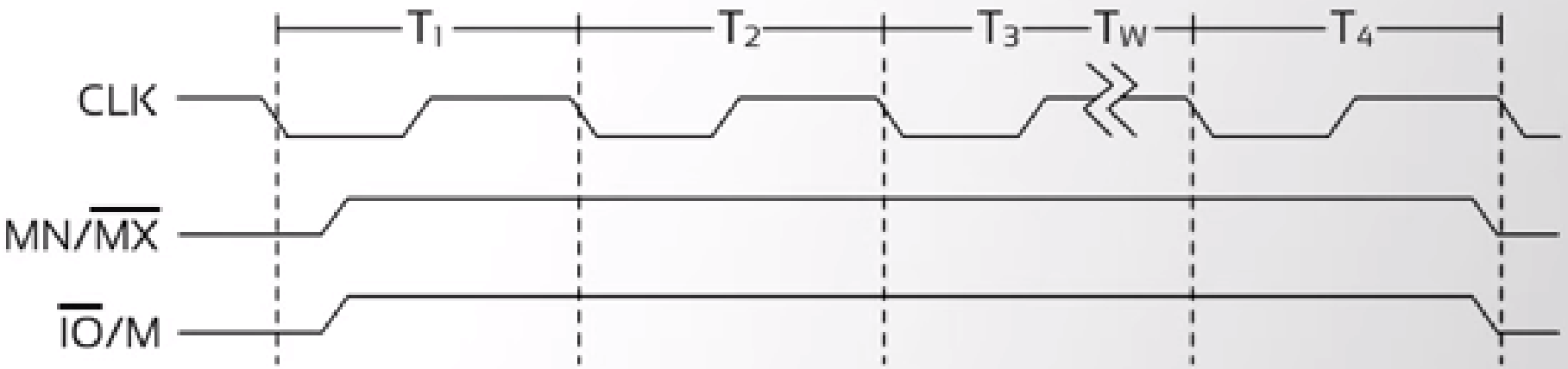
MN stands for Minimum mode.
MX stands for Maximum mode.

Timing Diagram for a read cycle

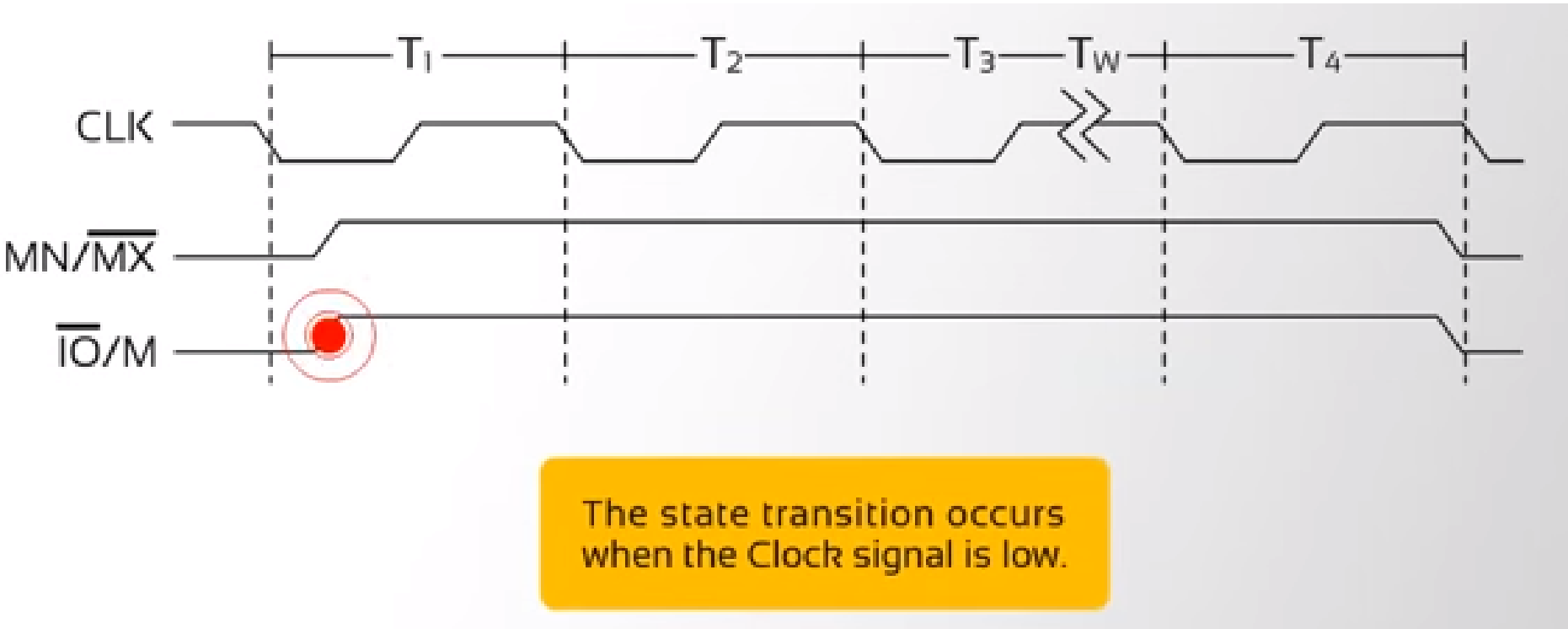


Timing Diagram for a read cycle

IO stands for Input/Output access.
M stands for Memory access.

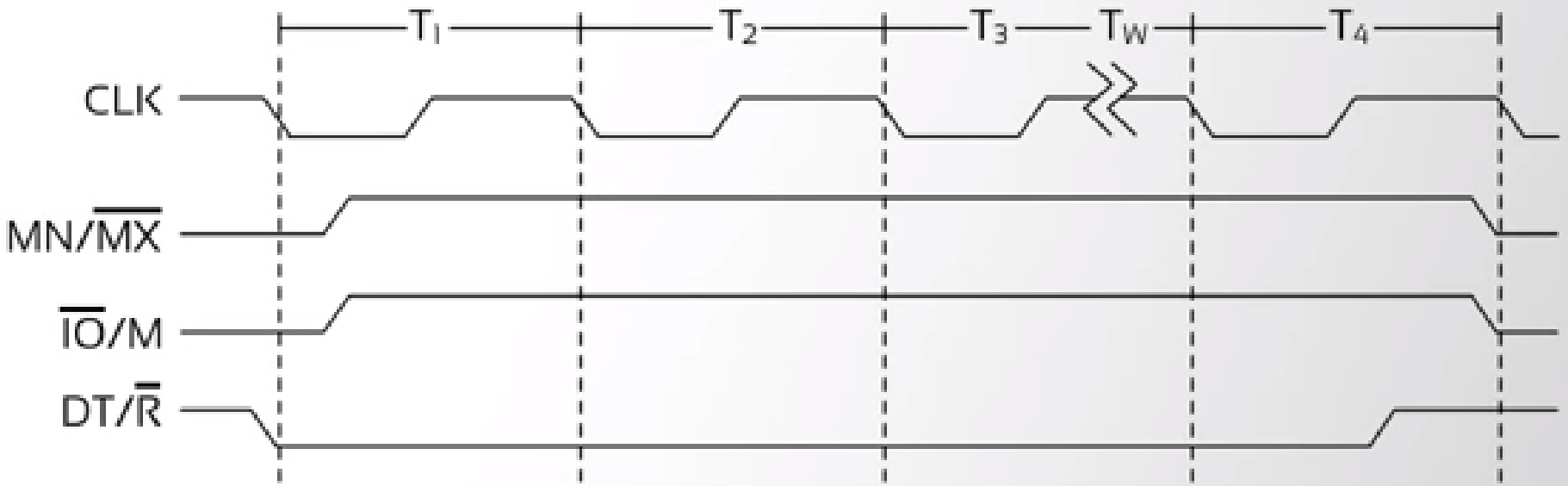


Timing Diagram for a read cycle

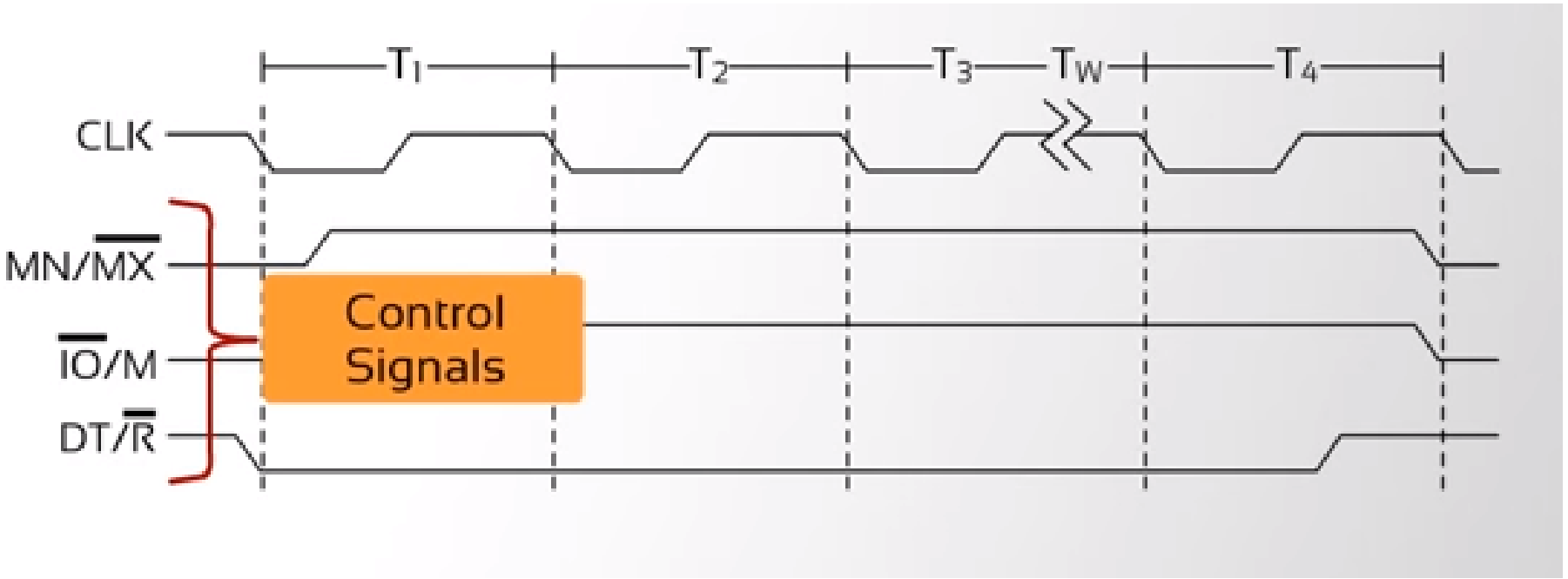


Timing Diagram for a read cycle

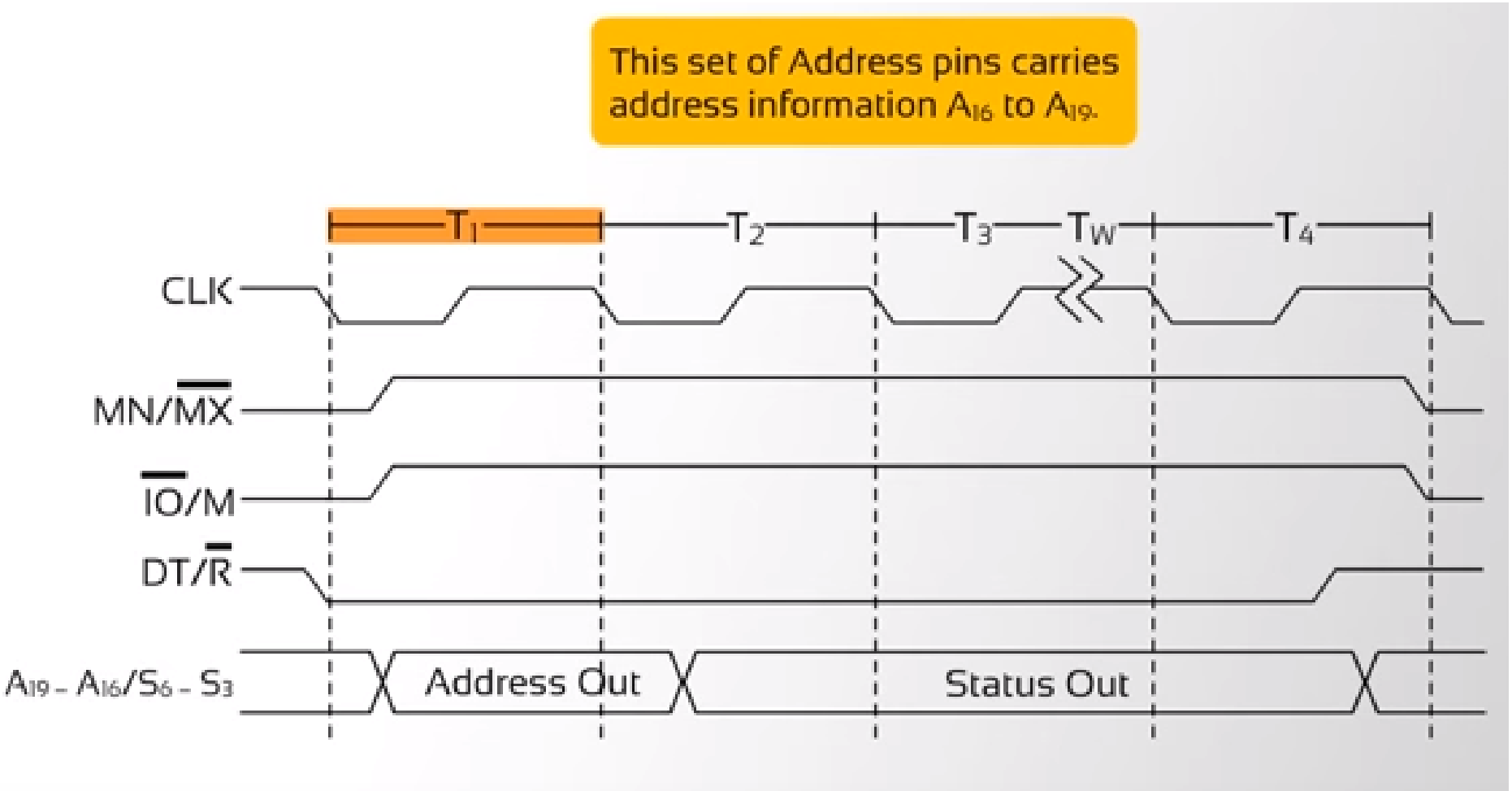
DT/R stands for Data Transmit (write)/Receive (read).



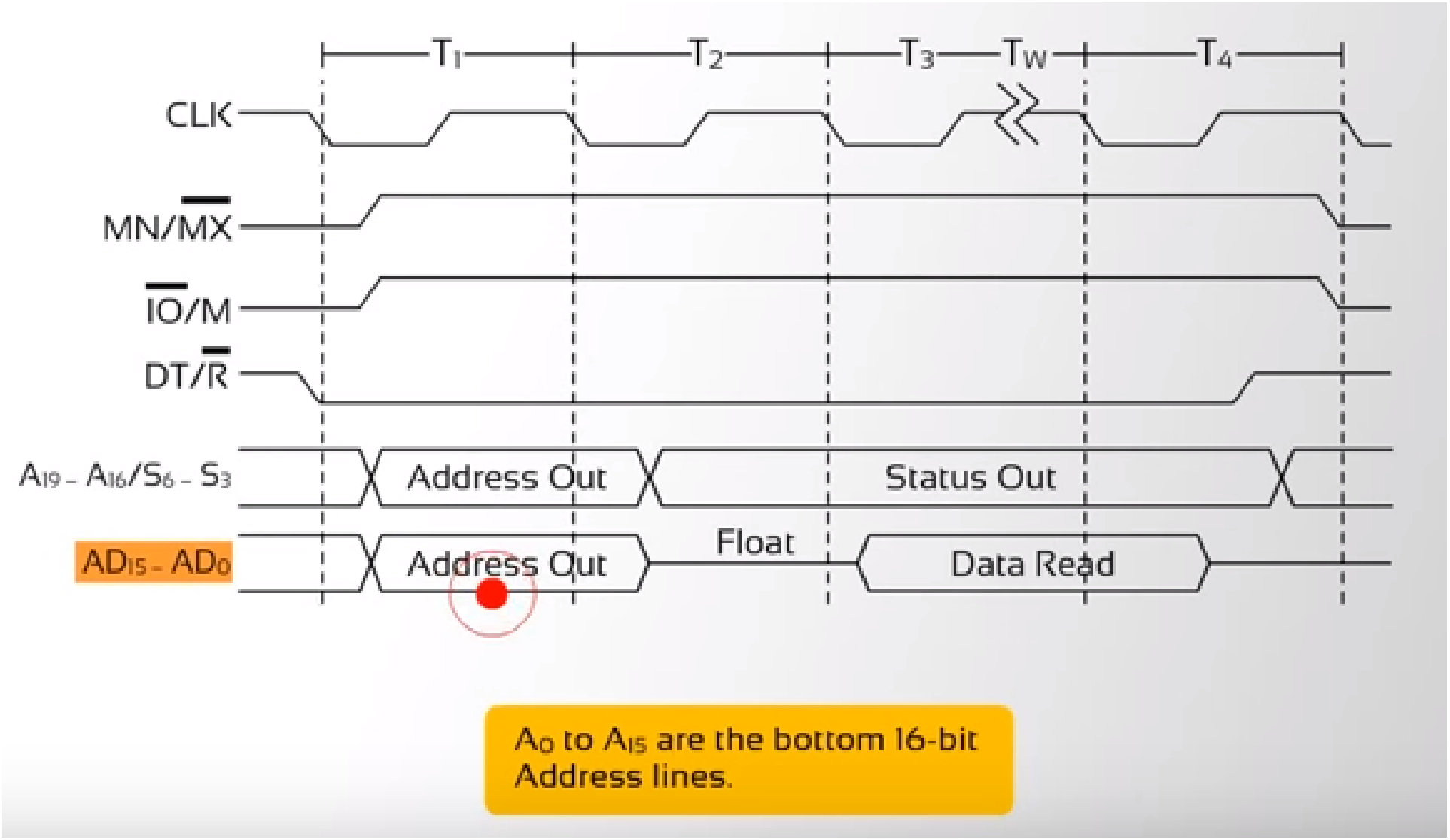
Timing Diagram for a read cycle



Timing Diagram for a read cycle



Timing Diagram for a read cycle



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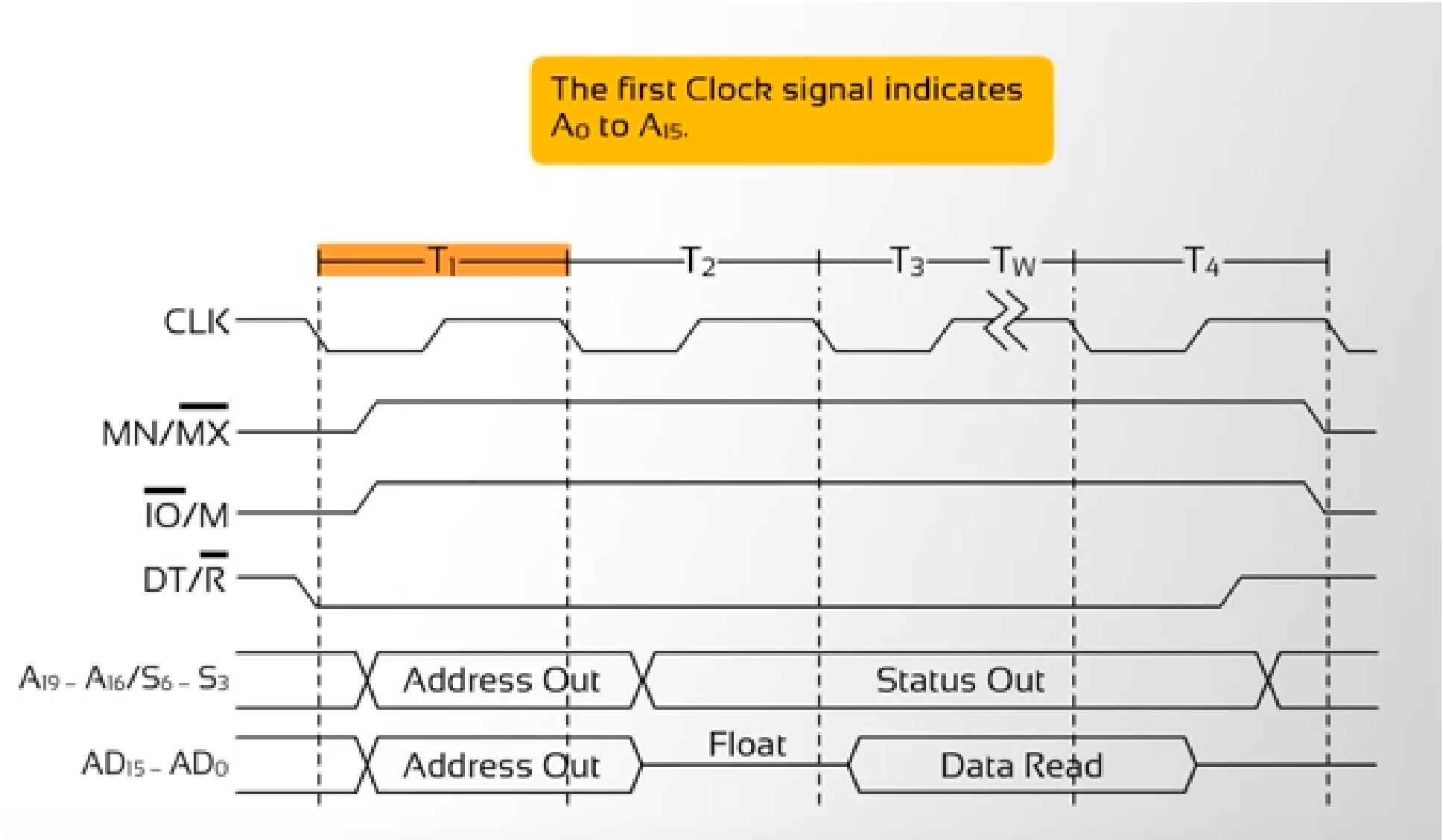

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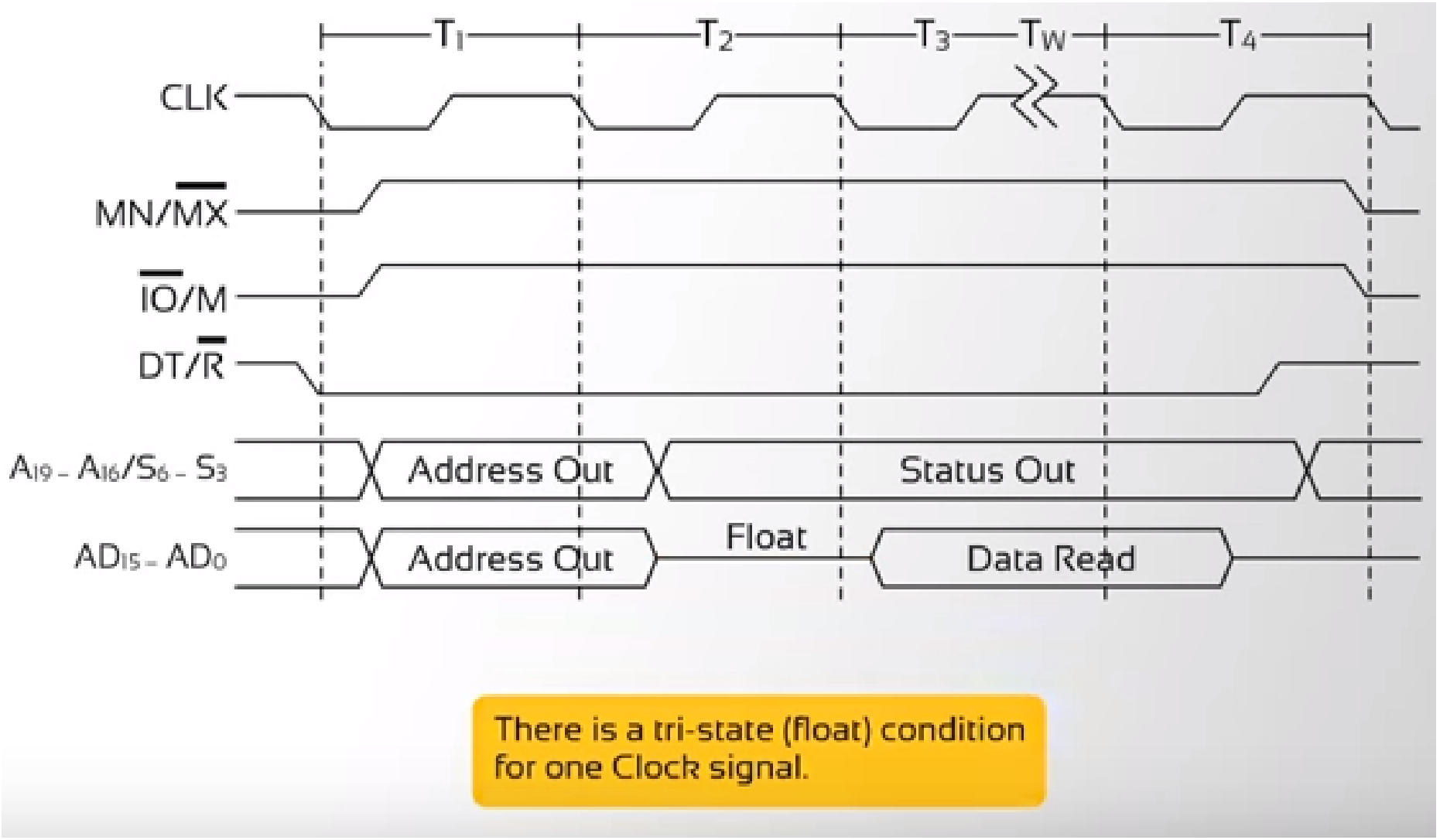

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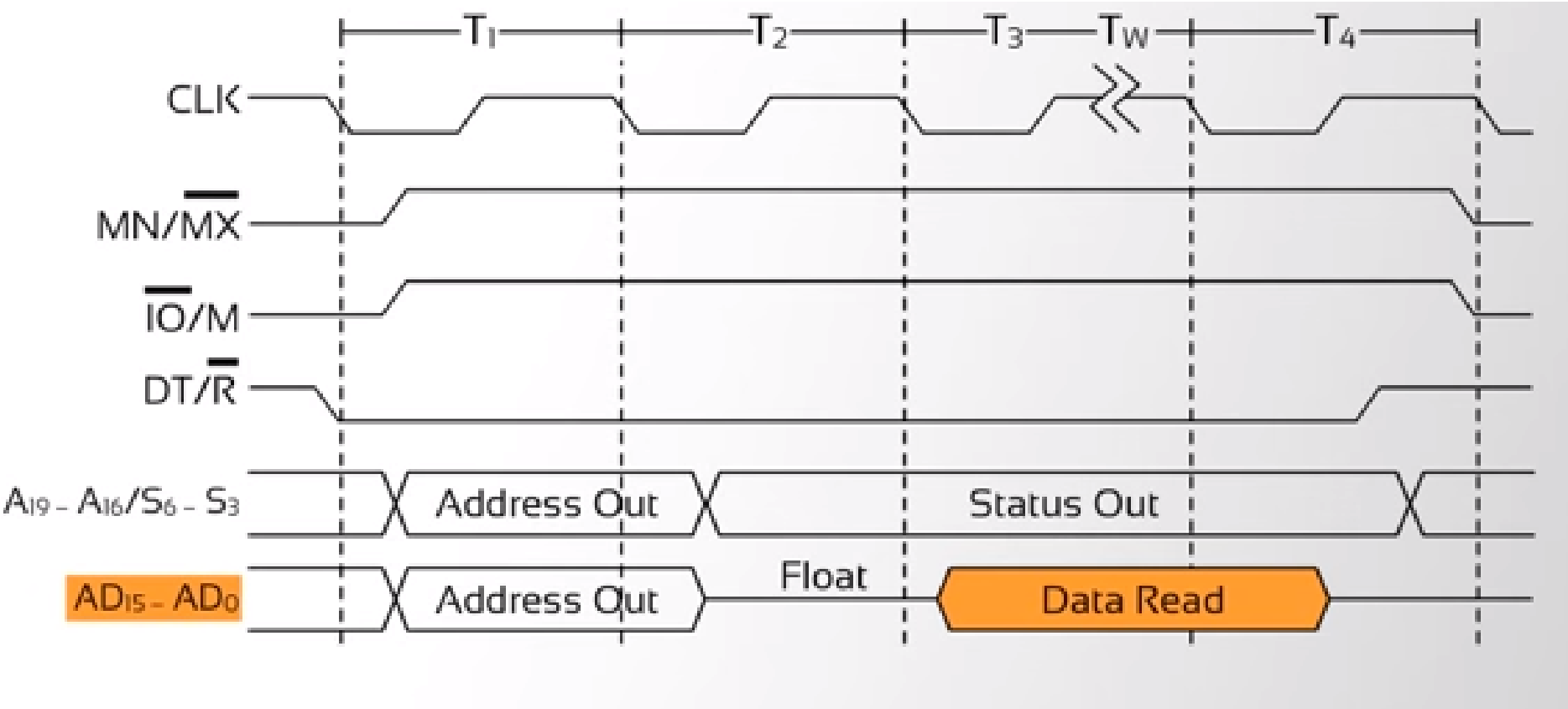

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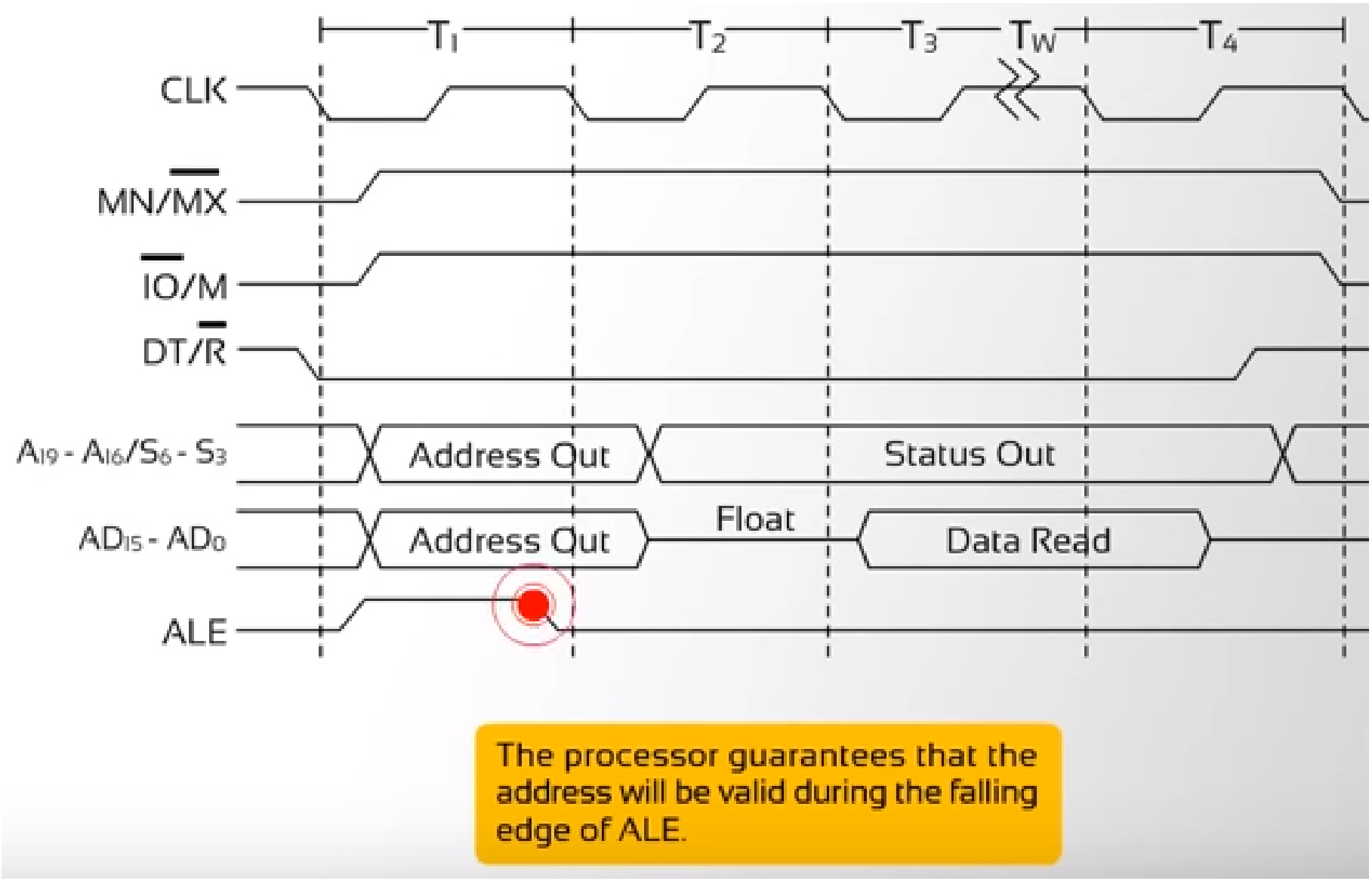

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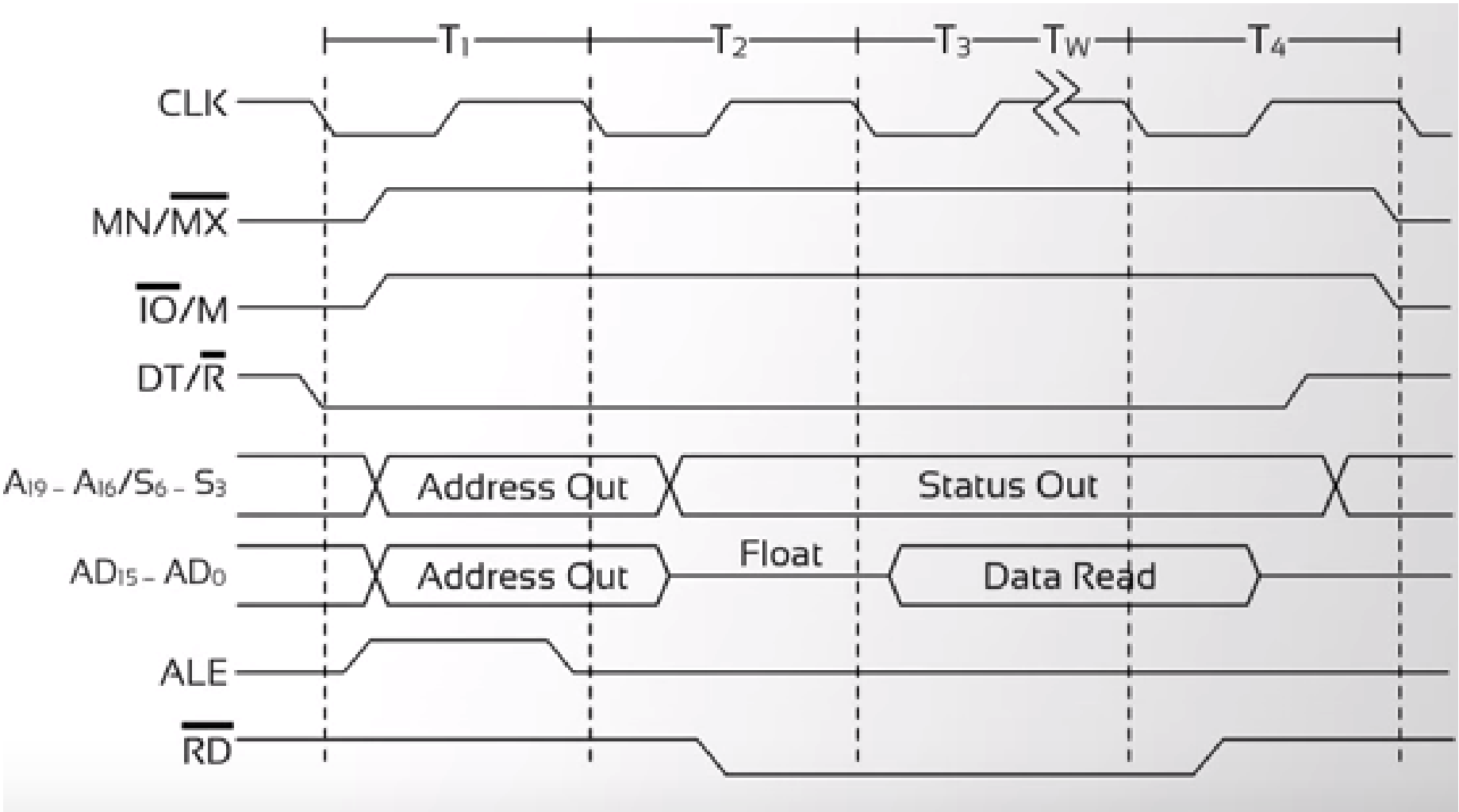

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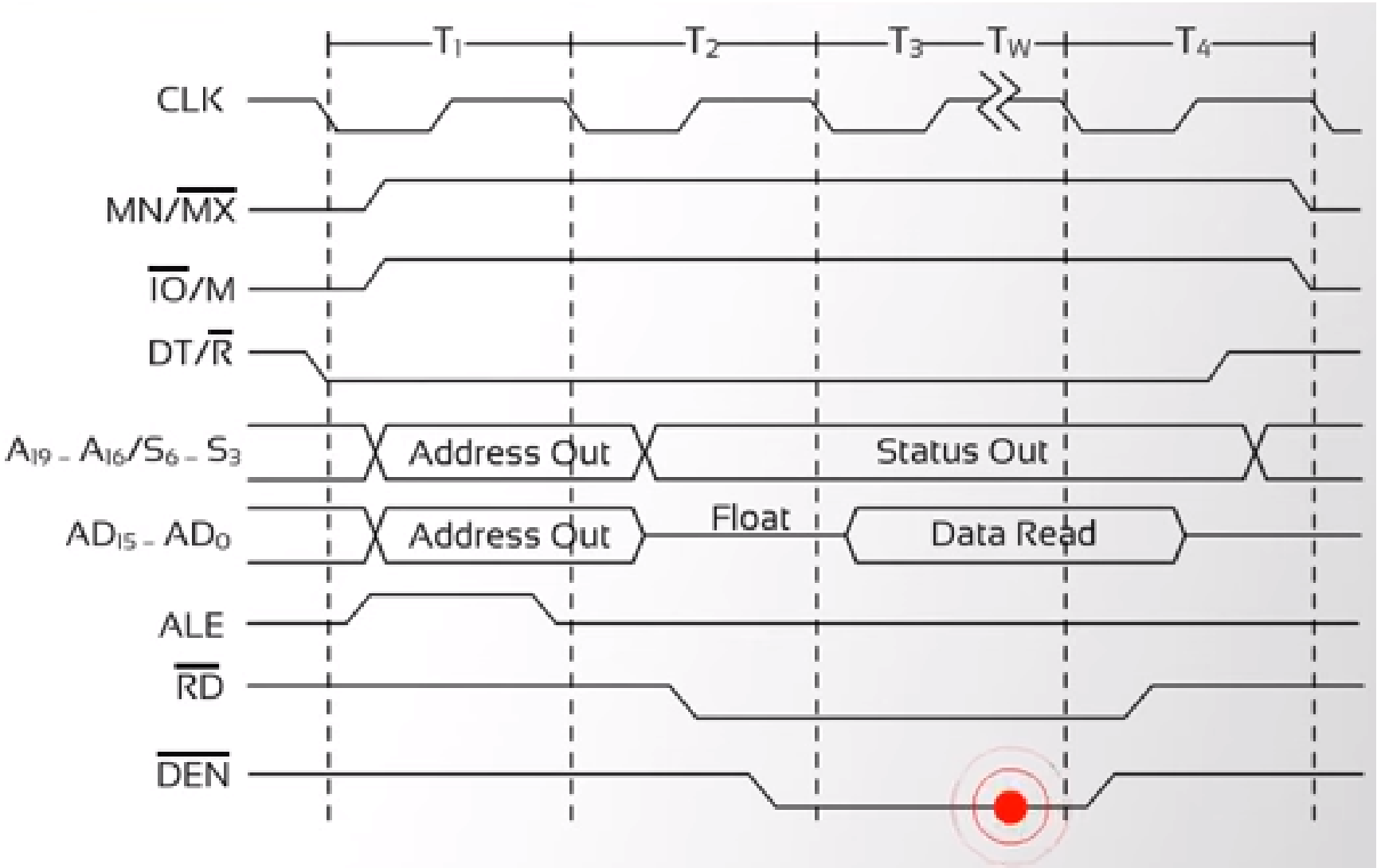
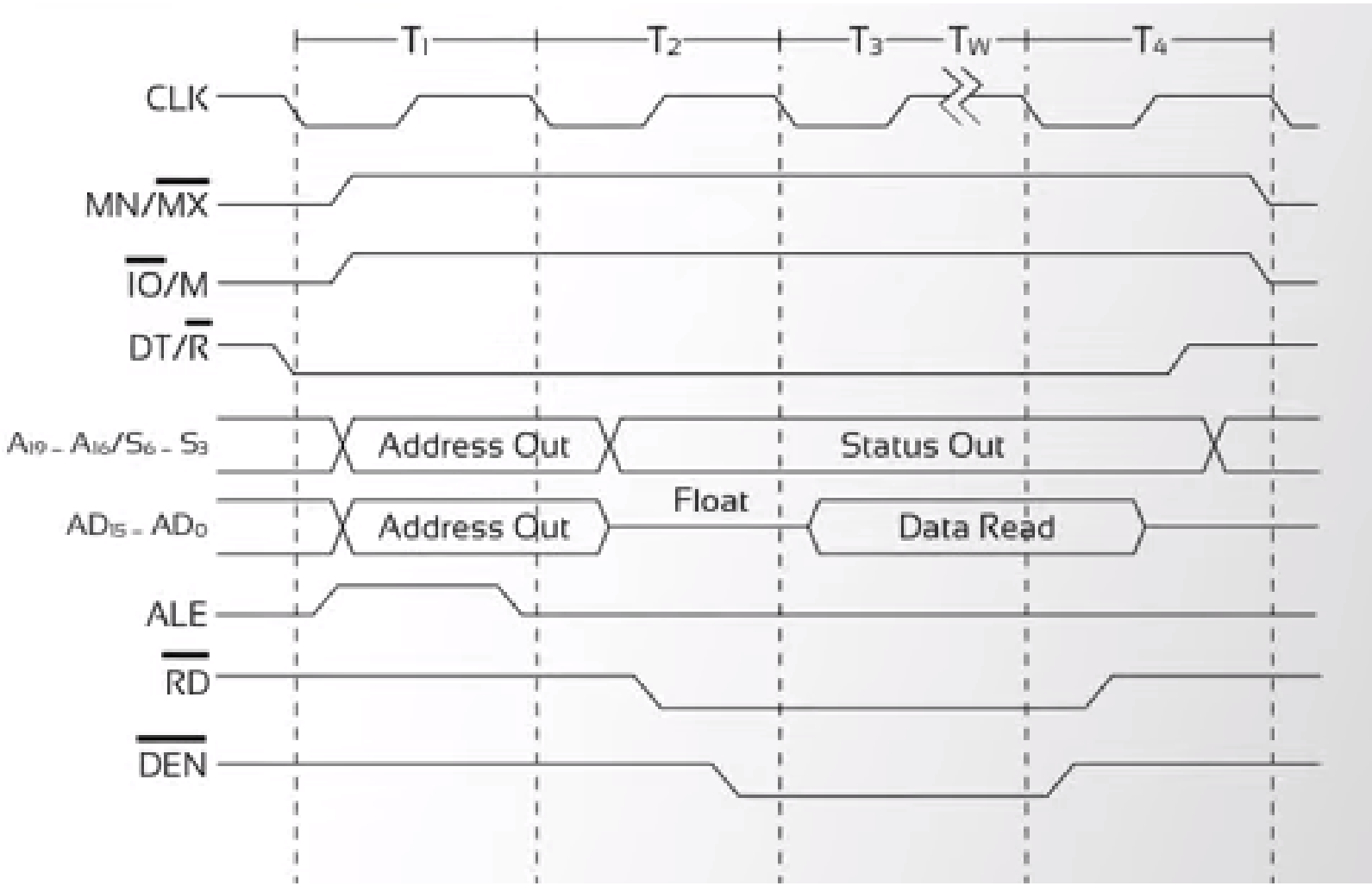


Period during which data is guaranteed by the processor during a Write Operation or it is read back during the Read Operation.

Timing Diagram for a read cycle



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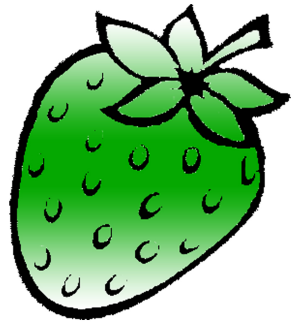

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