STRAWBERRY

/strawberrydevelopers
/twitter
/strawberry_app

For more visit:
Strawberrydevelopers.weebly.com
**Definition:** one discrete information transfer on bus
Also defined as time taken by processor to execute an instruction

Typically, all processors utilize the following 5 stage cycles:

- Fetch instruction from main memory
- Decode the instruction
- Fetch data from main memory
- Execute Instruction
- Store result
MACHINE CYCLE or BUS CYCLE or INSTRUCTION CYCLE

- All these operations are performed w.r.t. CLOCK
- Microprocessor performs an operation in a specific time period i.e. specific clock cycles known as \textbf{T-state}
- T-state is time period of a single cycle of the clock frequency
No. of T-state required to access a peripheral is called MACHINE CYCLE

Access a peripheral means to perform a read or a write operation either from memory or an I/O. In 8086 Memory read or memory write require 4 T-states.
Timing Diagram for a read cycle
Timing Diagram for a read cycle

$T_w$ stands for $T_{\text{wait}}$. 

CLK $T_1$ $T_2$ $T_3$ $T_w$ $T_4$
Timing Diagram for a read cycle

MN stands for Minimum mode.
MX stands for Maximum mode.
Timing Diagram for a read cycle

The state transition occurs when the Clock signal is low.
Timing Diagram for a read cycle

IO stands for Input/Output access. M stands for Memory access.
Timing Diagram for a read cycle

The state transition occurs when the Clock signal is low.
DT/R stands for Data Transmit (write)/Receive (read).

The image shows a timing diagram for a read cycle. The signals represented are:

- **CLK**
- **MN/MX**
- **IO/M**
- **DT/R**
Timing Diagram for a read cycle
Timing Diagram for a read cycle

This set of Address pins carries address information A₁₆ to A₁₉.

<table>
<thead>
<tr>
<th>CLK</th>
<th>MN/MX</th>
<th>IO/M</th>
<th>DT/R</th>
<th>A₁₉ – A₁₆/S₆ – S₃</th>
<th>Address Out</th>
<th>Status Out</th>
</tr>
</thead>
</table>
Timing Diagram for a read cycle

A₀ to A₁₅ are the bottom 16-bit Address lines.
Timing Diagram for a read cycle

The first Clock signal indicates $A_0$ to $A_{15}$.

- **T1**: Address Out
- **T2**: Status Out
- **T3**: Float
- **T4**: Data Read
Timing Diagram for a read cycle

There is a tri-state (float) condition for one Clock signal.
Timing Diagram for a read cycle
The processor guarantees that the address will be valid during the falling edge of ALE.
Timing Diagram for a read cycle

- CLK
- MN/MX
- IO/M
- DT/R
- A_{19} - A_{16}/S_6 - S_3
- A_{15} - A_0
- ALE
- RD

T_1 - T_2 - T_3 - T_W - T_4

Address Out
Status Out
Address Out
Float
Data Read
Timing Diagram for a read cycle

Period during which data is guaranteed by the processor during a Write Operation or it is read back during the Read Operation.
Timing Diagram for a read cycle

- **CLK**
- **MN/MX**
- **IO/M**
- **DT/R**
- **A19 - A16, S6 - S3:** Address Out
- **AD15 - AD0:** Address Out, Float, Data Read
- **ALE**
- **RD**
- **DEN**

Addresses:

- **A19 - A16:** S6 - S3
- **ADC**
- **AD0**

Timing phases:

- **T1**
- **T2**
- **T3**
- **T_W**
- **T4**
STRAWBERRY

/strawberrydevelopers
/tWSTRawberry_app

For more visit:
Strawberrydevelopers.weebly.com