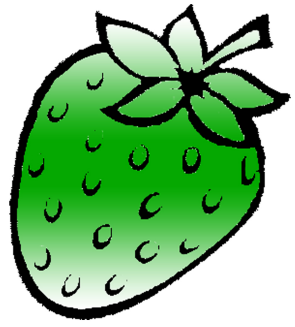
STRAWBERRY



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PIN DIAGRAM

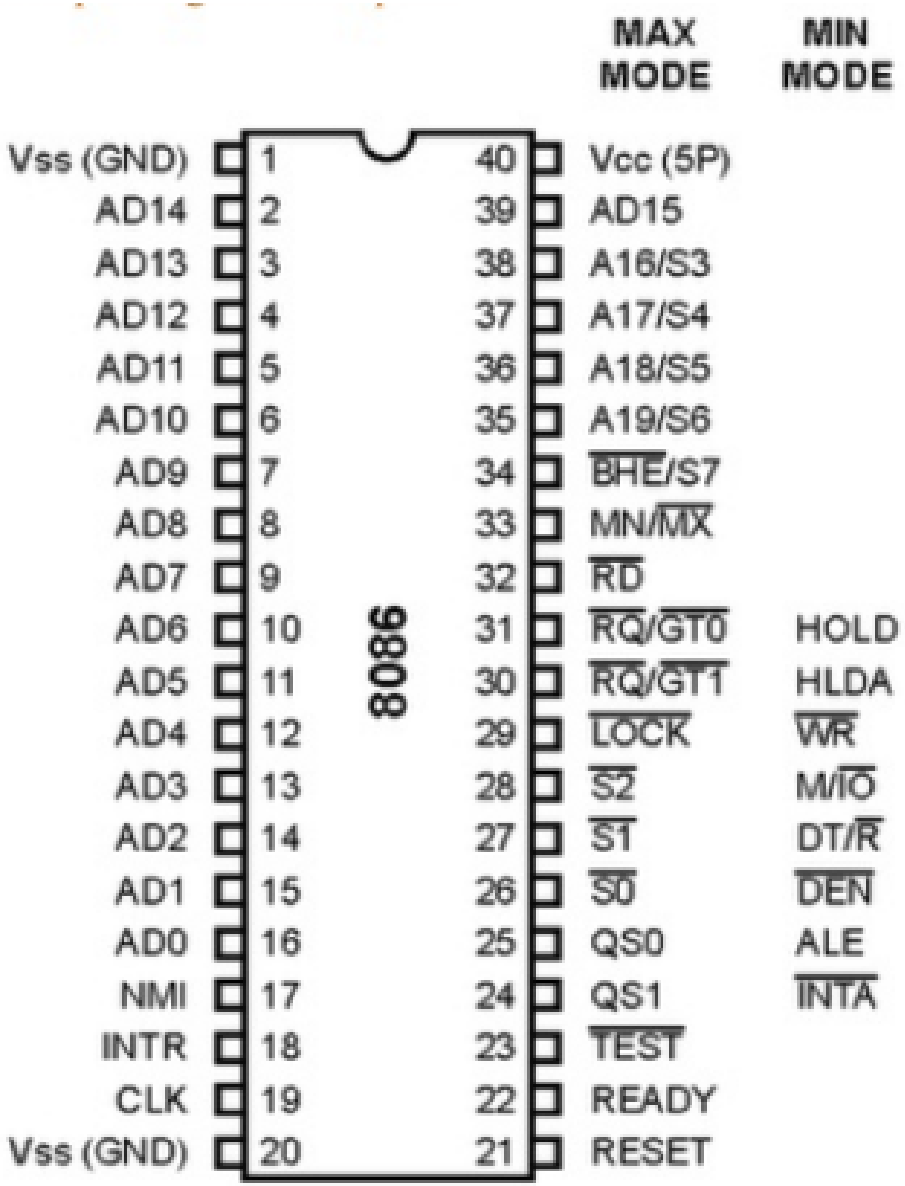
Richa Upadhyay Prabhu

NMIMS's MPSTME

richa.upadhyay@nmims.edu

January 19, 2016

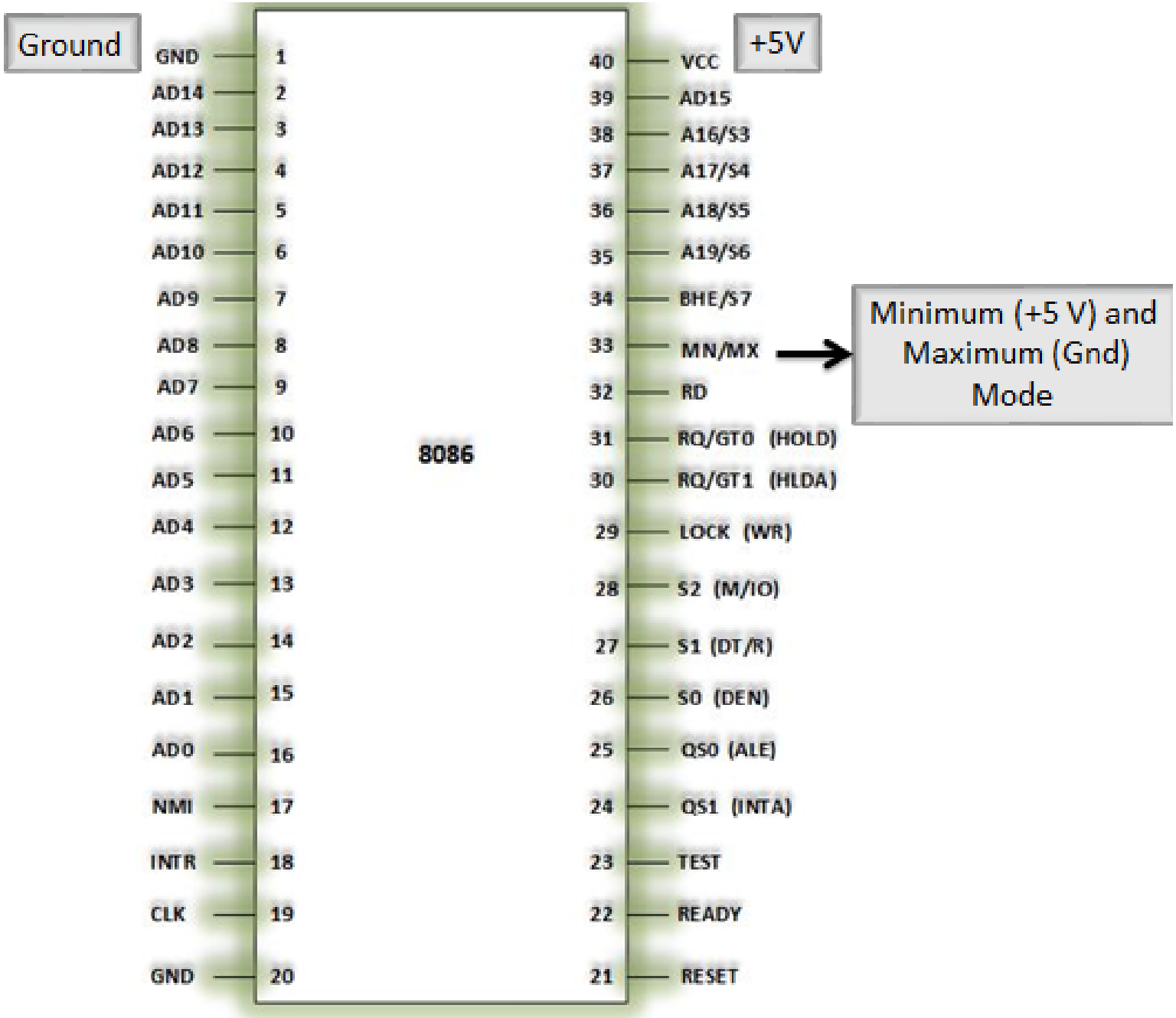
Pin Diagram of 8086



Pin Diagram of 8086

8086 can operate in two modes :

- Minimum Mode : unique processor system with a single 8086
- Maximum Mode : multiprocessor system with more than one 8086


Ground
GND 1
AD14 2
AD13 3
AD12 4
AD11 5
AD10 6
AD9 7
AD8 8
AD7 9
AD6 10
AD5 11
AD4 12
AD3 13
AD2 14
AD1 15
AD0 16
NMI 17
INTR 18
CLK 19
GND 20
8086
40 VCC
+5V
39 AD15
38 A16/S3
37 A17/S4
36 A18/S5
35 A19/S6
34 BHE/S7
33 MN/MX
32 RD
31 RQ/GT0 (HOLD)
30 RQ/GT1 (HLDA)
29 LOCK (WR)
28 S2 (M/IO)
27 S1 (DT/R)
26 S0 (DEN)
25 QS0 (ALE)
24 QS1 (INTA)
23 TEST
22 READY
21 RESET
Minimum (+5 V) and Maximum (Gnd) Mode

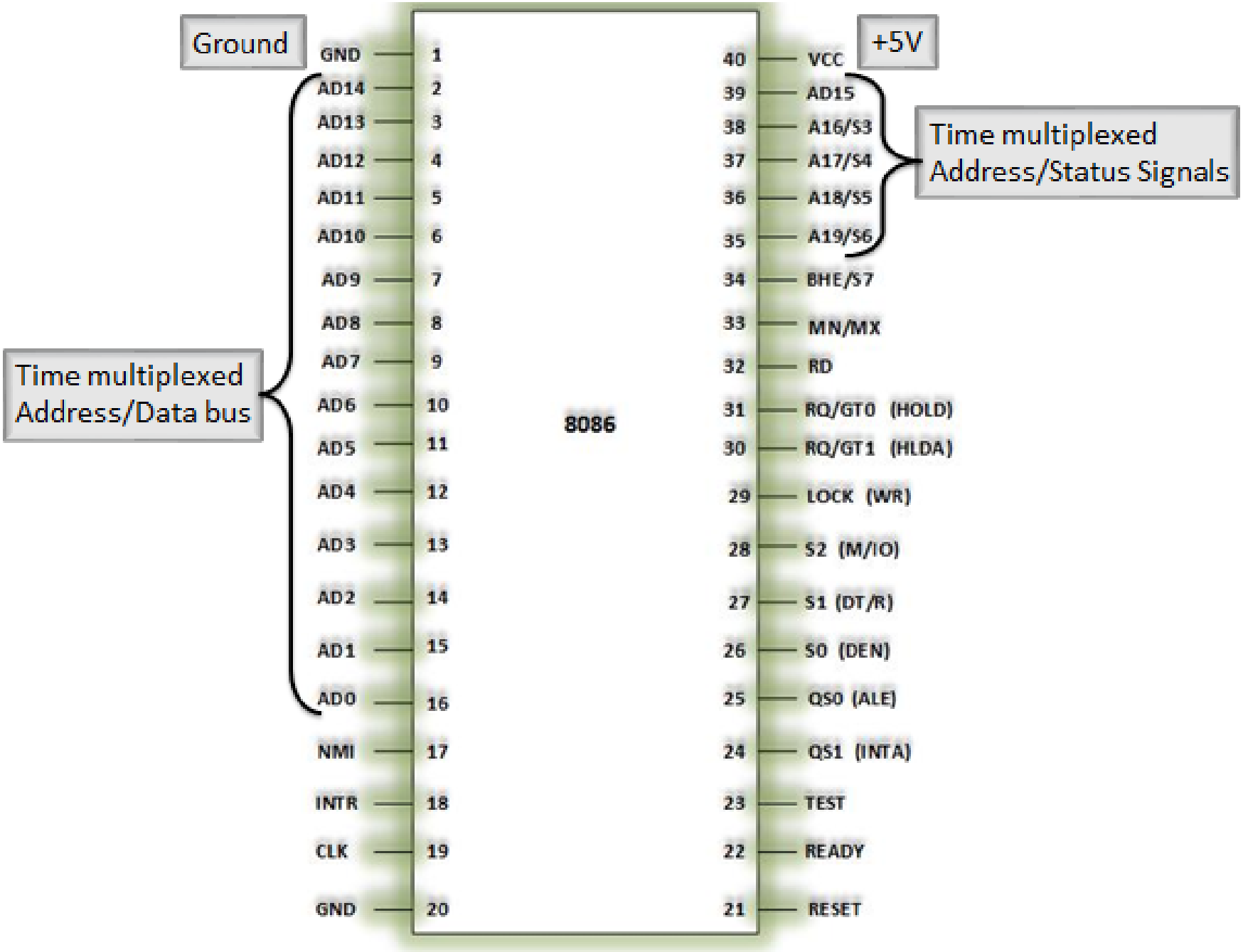
Pin Diagram of 8086

Minimum mode

- Pin 33 (MN/MX) connect to +5V
- Pin 24-31 are used as memory and I/O control signal
- The control signals are generated internally by the 8086/88

Maximum mode

- Pin 33 (MN/MX) connect to Ground
- Some control signals are generated externally by the 8288 bus controller chip
- Max mode is used when math processor is used.


Ground
GND 1
AD14 2
AD13 3
AD12 4
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AD10 6
AD9 7
AD8 8
AD7 9
AD6 10
AD5 11
AD4 12
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AD2 14
AD1 15
AD0 16
NMI 17
INTR 18
CLK 19
GND 20
Time multiplexed
Address/Data bus
8086
40 VCC
39 AD15
38 A16/S3
37 A17/S4
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35 A19/S6
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33 MN/MX
32 RD
31 RQ/GT0 (HOLD)
30 RQ/GT1 (HLDA)
29 LOCK (WR)
28 S2 (M/IO)
27 S1 (DT/R)
26 S0 (DEN)
25 QS0 (ALE)
24 QS1 (INTA)
23 TEST
22 READY
21 RESET
+5V
Time multiplexed
Address/Status Signals

Pin Diagram of 8086

$AD_{15} - AD0$: Address Data Bus

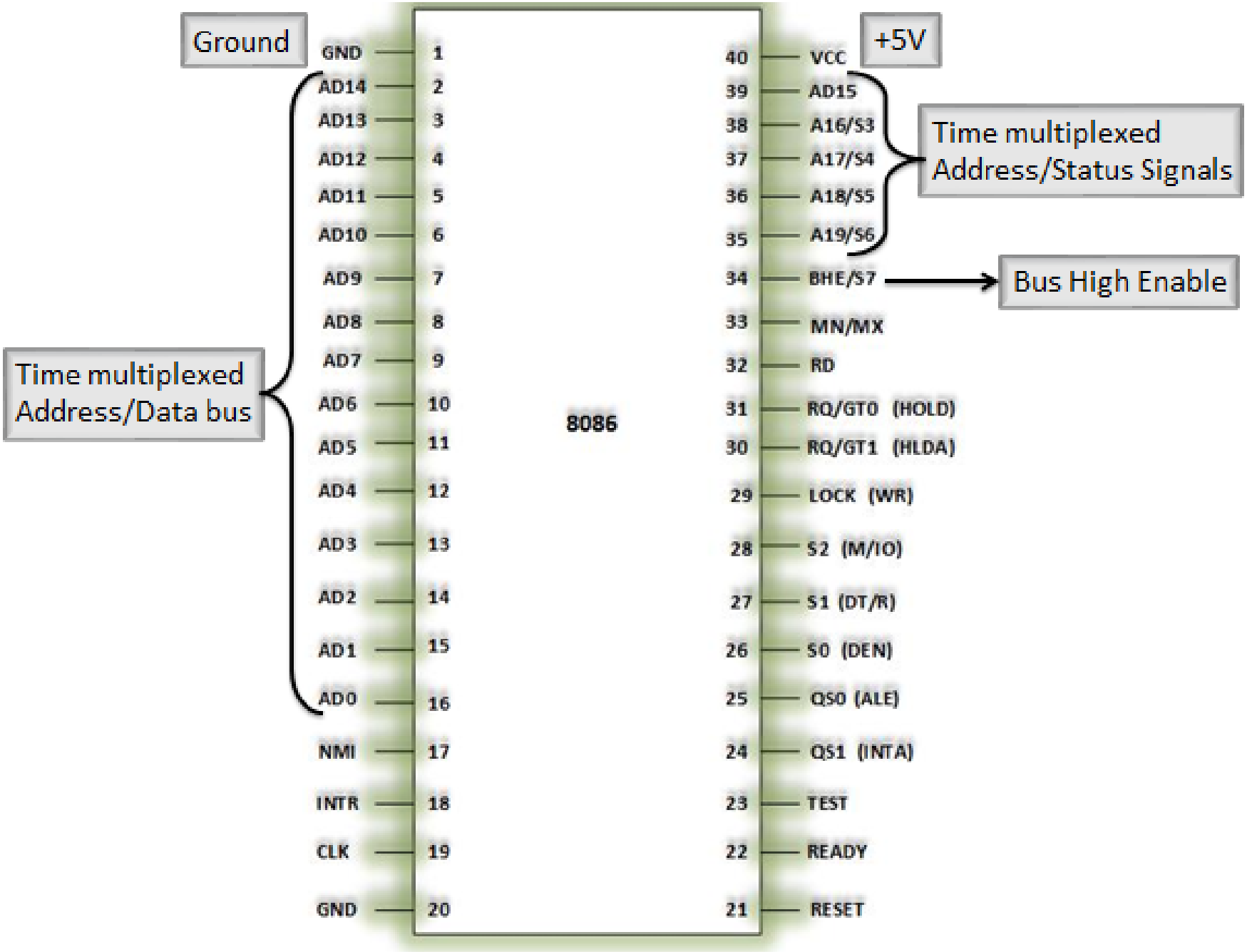
- 16-bit multiplexed address and data bus
- During the 1st clock cycle $AD_0 - AD_{15}$ are the low order 16-Bit address
- The 8086 has a total of 20 address line ,the upper 4 lines are multiplexed with the state signal that is $A_{16}/S_3, A_{17}/S_4, A_{18}/S_5, A_{19}/S_6$.
- During the first clock period the entire 20-bit address is available on these line
- In the next cycle, $AD_{15} - AD_0$ contain the 16 bit data and S3,S4,S5,S6 become the status line

Pin Diagram of 8086

S_3 and S_4 are decoded as follows

- 00 extra segment
- 01 stack segment
- 10 code or no segment
- 11 data segment

After the first clock cycle of an instruction execution, the A_{17}/S_4 andA_{16}/S_3 pins specify which segment register generates the segment portion of the 8086 address.


Ground
GND 1
AD14 2
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AD12 4
AD11 5
AD10 6
AD9 7
AD8 8
AD7 9
AD6 10
AD5 11
AD4 12
AD3 13
AD2 14
AD1 15
AD0 16
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Time multiplexed Address/Data bus
8086
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+5V
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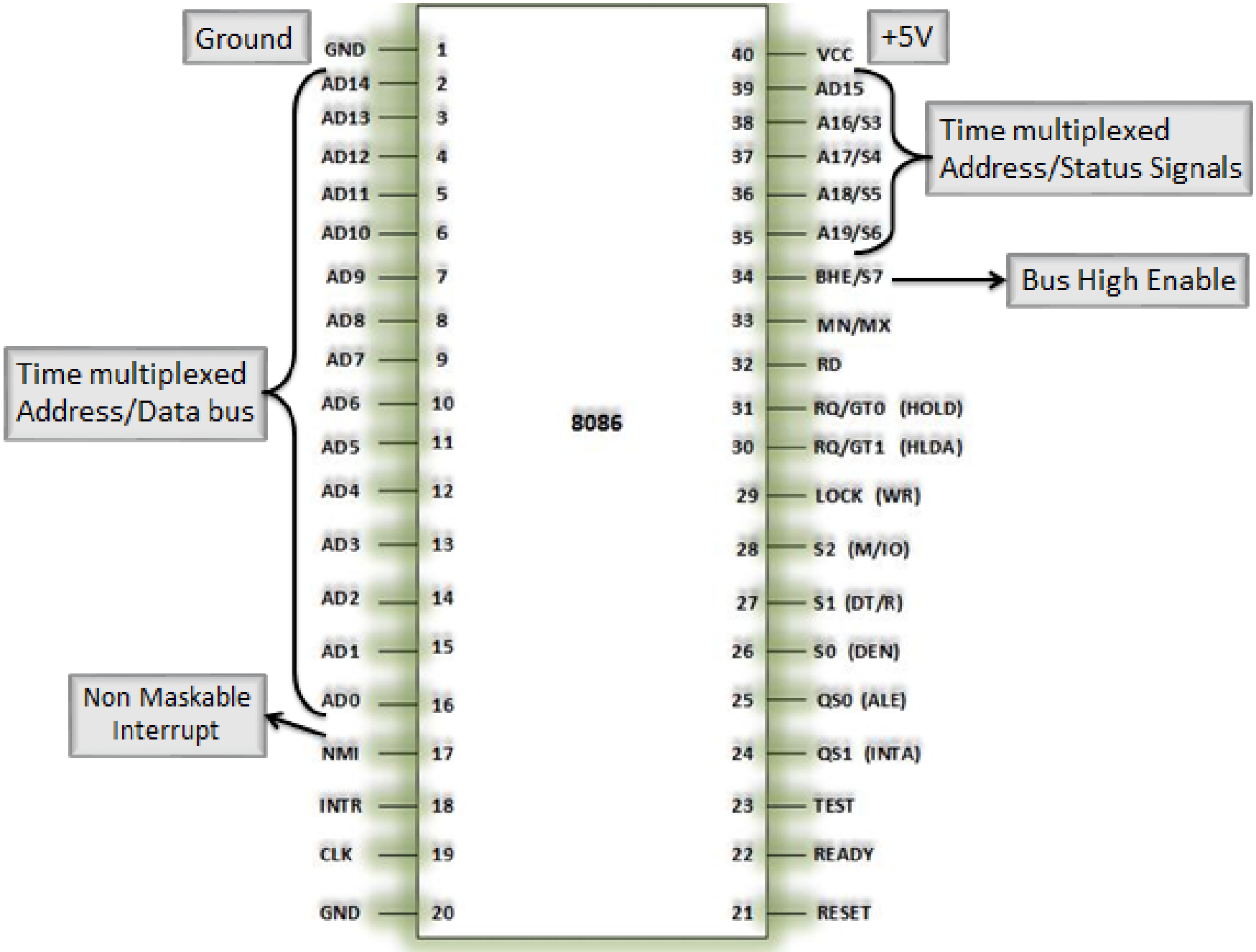
35 A19/S6
Time multiplexed Address/Status Signals
34 BHE/S7
Bus High Enable
33 MN/MX
32 RD
31 RQ/GT0 (HOLD)
30 RQ/GT1 (HLDA)
29 LOCK (WR)
28 S2 (M/IO)
27 S1 (DT/R)
26 S0 (DEN)
25 QS0 (ALE)
24 QS1 (INTA)
23 TEST
22 READY
21 RESET

BHE/S_7: is used as bus high enable during the 1st clock cycle of an instruction execution

- Used to enable data on the most significant half of data bus
- or can say used to distinguish between the low byte and the high byte of the data for the 16-bit external data bus of 8086
- BHE is Low during T1 state of read, write and interrupt acknowledge cycles when a byte is to be transferred on the high portion of the bus.

BHE	AD0		
0	0	16-bit	D0-D15
0	1	8-bit	Upper half, D8-D15
1	0	8-bit	Lower half, D0-D7
1	1		Data Bus Idle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GND 1
AD14 2
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AD12 4
AD11 5
AD10 6
AD9 7
AD8 8
AD7 9
AD6 10
AD5 11
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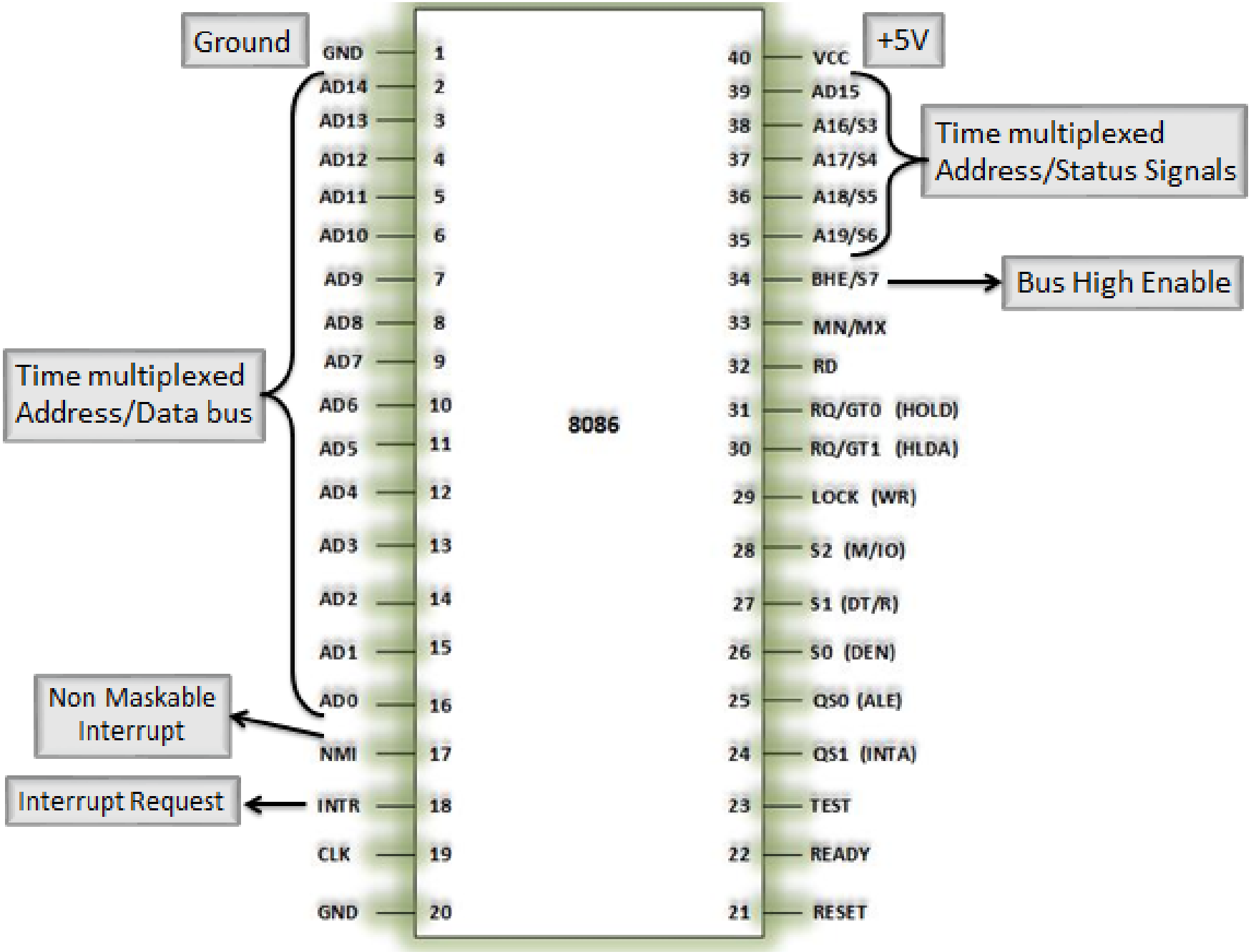
27 S1 (DT/R)
26 S0 (DEN)
25 QS0 (ALE)
24 QS1 (INTA)
23 TEST
22 READY
21 RESET
+5V
Time multiplexed Address/Status Signals
Bus High Enable
Time multiplexed Address/Data bus
Non Maskable Interrupt

NMI : Non Maskable Interrupt; An edge triggered input, causes a type-2 interrupt.

- A subroutine is vectored to via the interrupt vector look up table located in system memory.
- NMI is not maskable internally by software.
- A transition from a LOW to HIGH on this pin initiates the interrupt at the end of the current instruction.
- This input is internally synchronized.


Ground
GND 1
AD14 2
AD13 3
AD12 4
AD11 5
AD10 6
AD9 7
AD8 8
AD7 9
AD6 10
AD5 11
AD4 12
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26 S0 (DEN)
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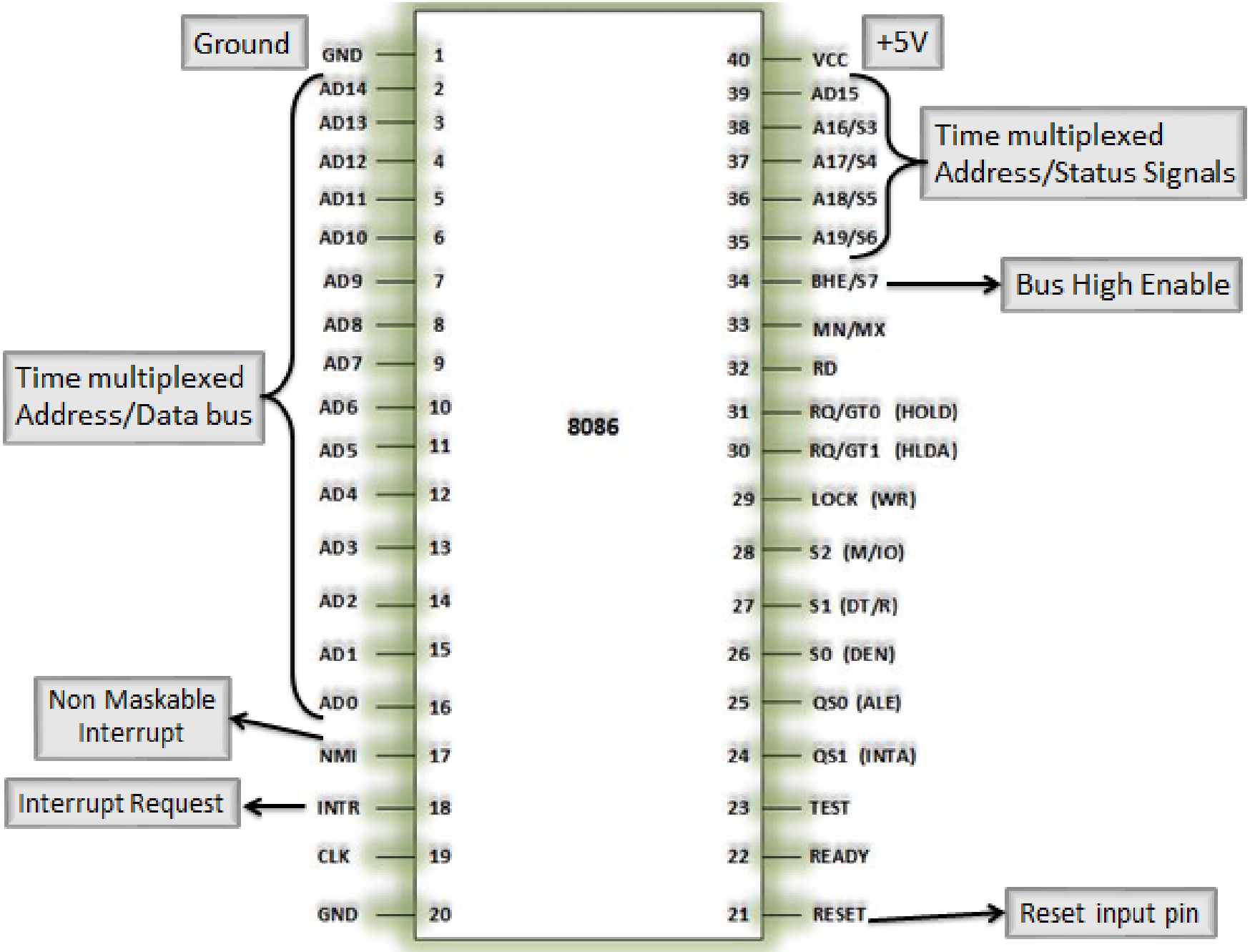
24 QS1 (INTA)
23 TEST
22 READY
21 RESET
+5V
Time multiplexed Address/Status Signals
Bus High Enable
Time multiplexed Address/Data bus
Non Maskable Interrupt
Interrupt Request

Pin Diagram of 8086

INTR (Interrupt Request)

- An active-high level-triggered input signal to the processor
- Sampled in the last clock cycle of each instruction
- In IBM PC, this is connected to the 8259 Interrupt controller


Ground
GND 1
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AD11 5
AD10 6
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AD8 8
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AD5 11
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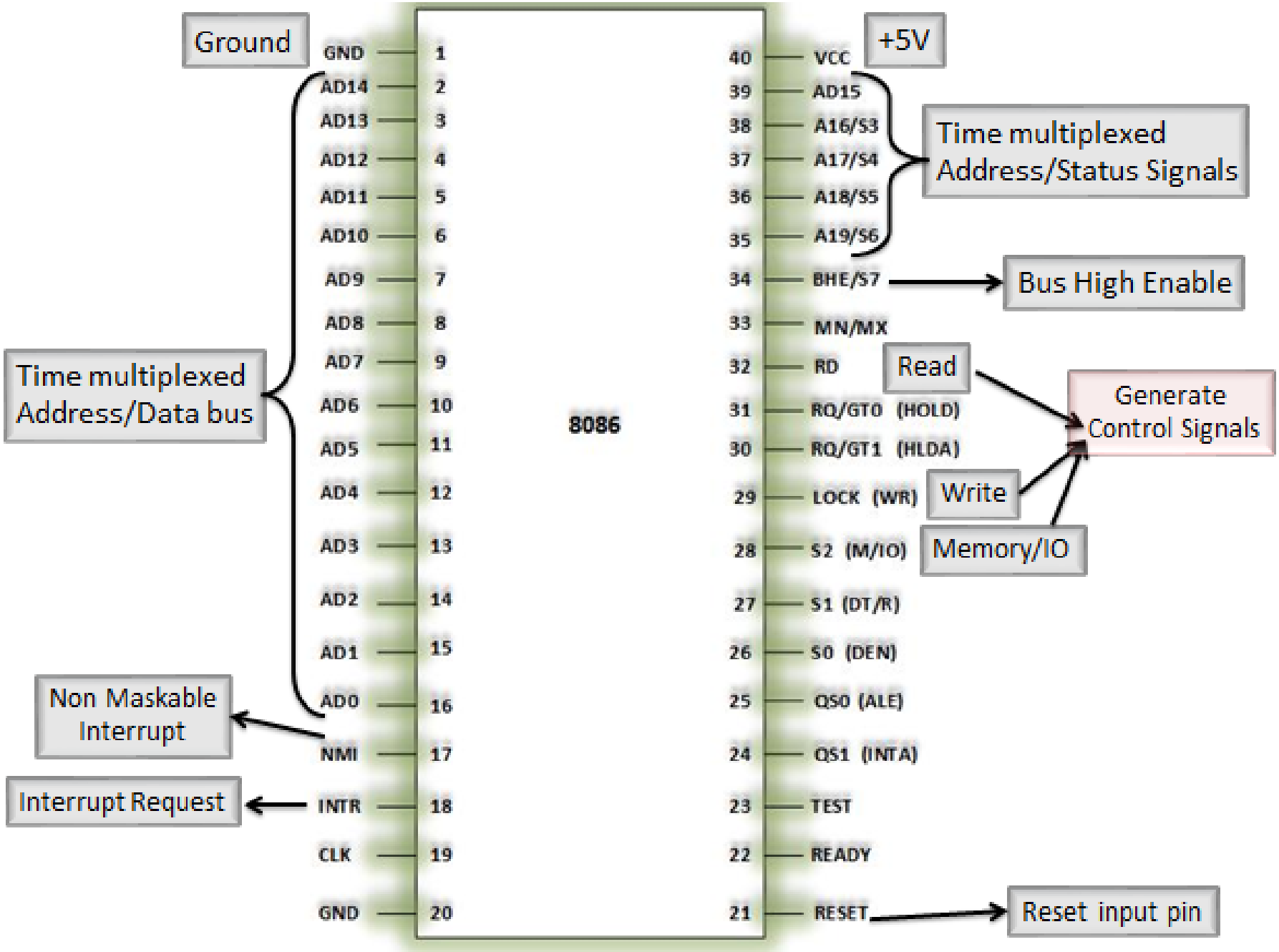
23 TEST
22 READY
21 RESET
+5V
Time multiplexed Address/Status Signals
Bus High Enable
Time multiplexed Address/Data bus
Non Maskable Interrupt
Interrupt Request
Reset input pin

Pin Diagram of 8086

RESET : causes the processor to immediately terminate its present activity

- Active high signal came from 8284
- Force the processor to stop any activities and to discard everything
- The signal must be active high for at least four clock cycles,
- Data after reset: CS: FFFFH, IP: 0000H, DS ES SS: 0000H Flags: Cleared, Queue: Empty


Ground
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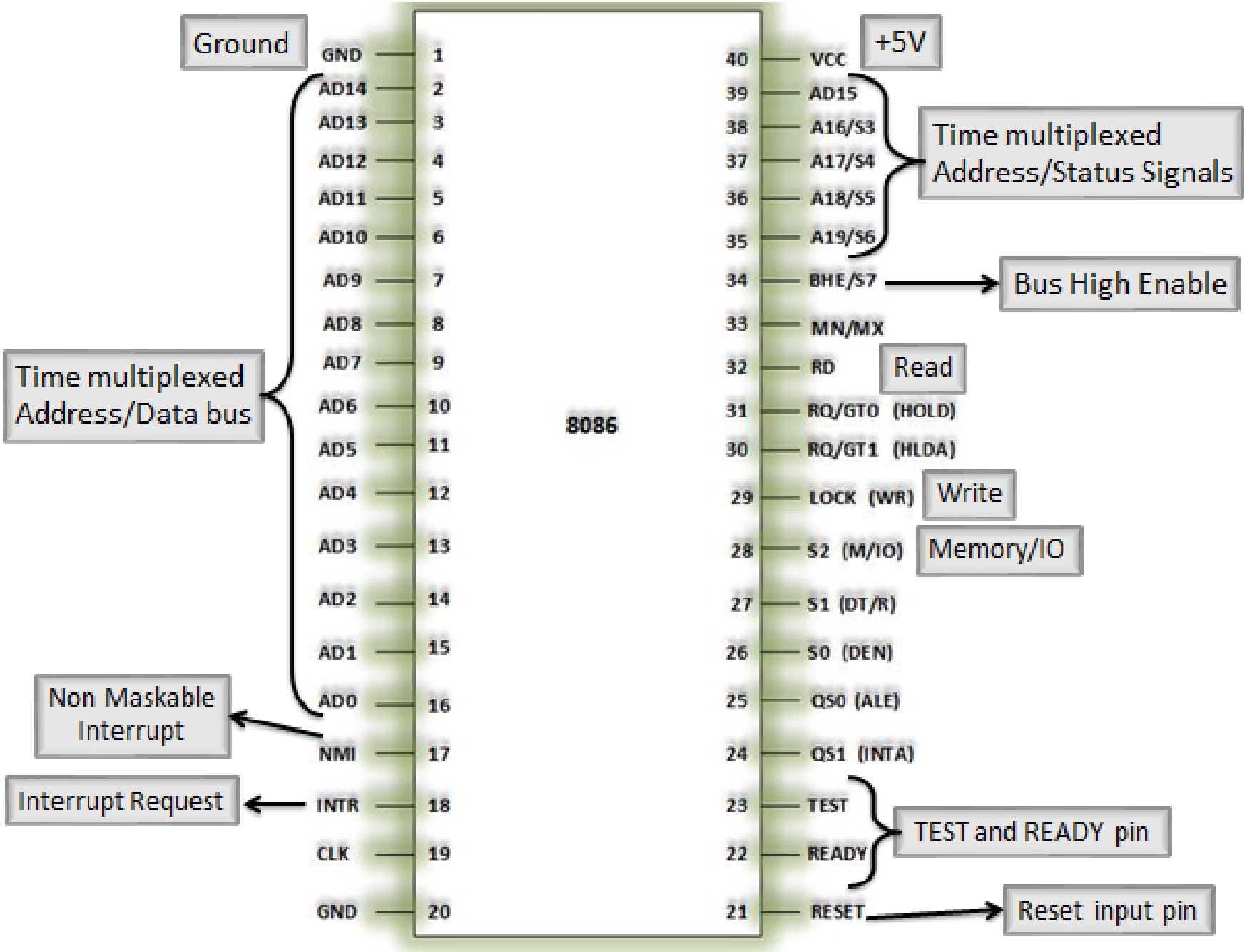
26 S0 (DEN)
25 QS0 (ALE)
24 QS1 (INTA)
23 TEST
22 READY
21 RESET
+5V
Time multiplexed Address/Status Signals
Bus High Enable
Read
Generate Control Signals
Write
Memory/IO
Time multiplexed Address/Data bus
Non Maskable Interrupt
Interrupt Request
Reset input pin

Generation of Control signals

using RD, WR and IO/M pins

RD	WR	IO/M	Signal
0	1	0	$\overline{\text{MEMR}}$
1	0	0	$\overline{\text{MEMW}}$
0	1	1	$\overline{\text{IOR}}$
1	0	1	$\overline{\text{IOW}}$
0	0	x	Never happens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24 QS1 (INTA)
23 TEST
22 READY
21 RESET
+5V
Time multiplexed Address/Status Signals
Bus High Enable
Read
Write
Memory/IO
TEST and READY pin
Reset input pin
Time multiplexed Address/Data bus
Non Maskable Interrupt
Interrupt Request

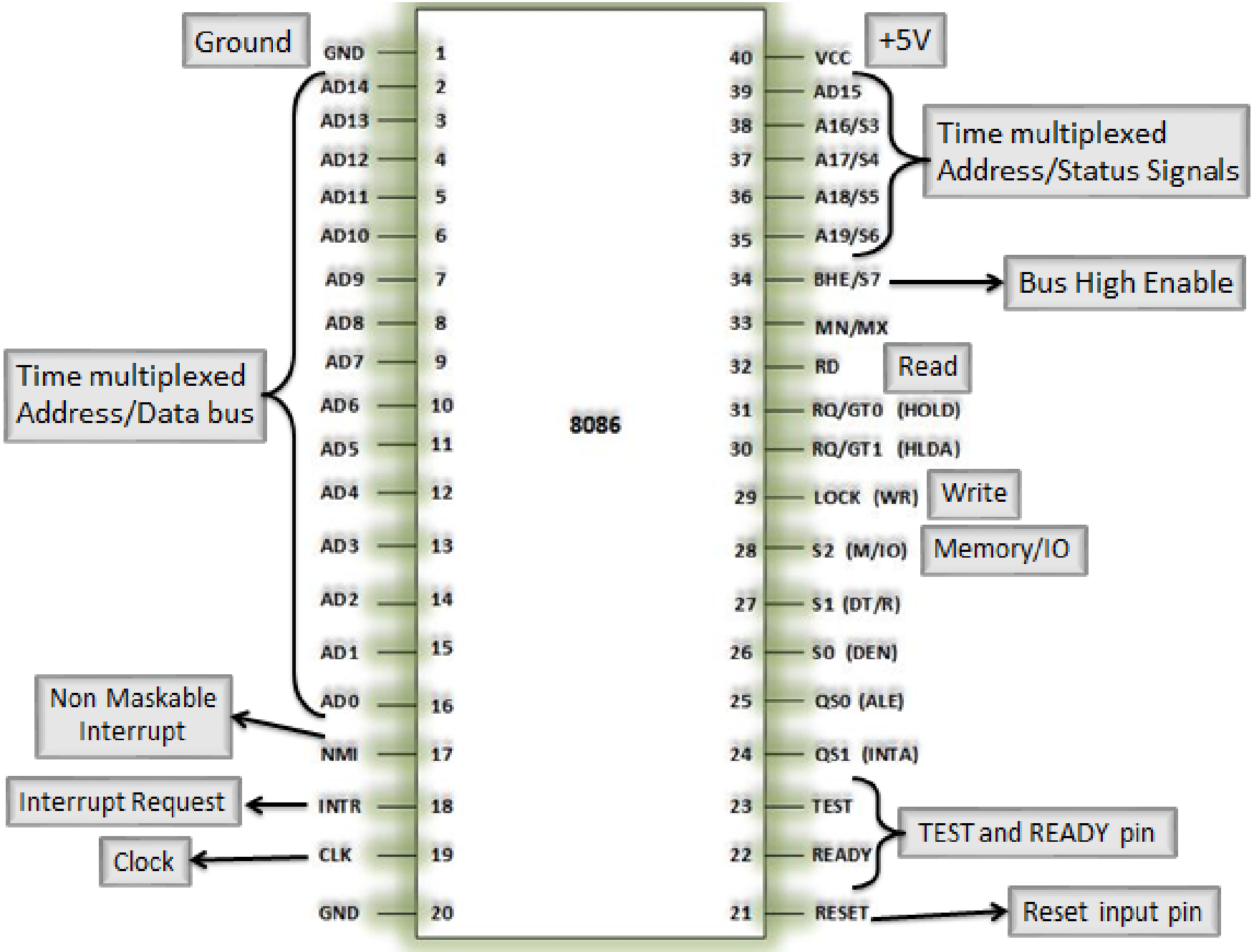
Pin Diagram of 8086

TEST

- TEST pin is examined by the "WAIT" instruction.
- If the TEST pin is Low, execution continues. Otherwise the processor waits in an "idle" state.
- This input is synchronized internally during each clock cycle on the leading edge of CLK.

READY

- is the acknowledgement from the addressed memory or I/O device that it has completed the data transfer.
- The READY signal from memory or I/O is synchronized by the 8284 clock generator to form READY.
- This signal is active HIGH.


Ground
GND 1
AD14 2
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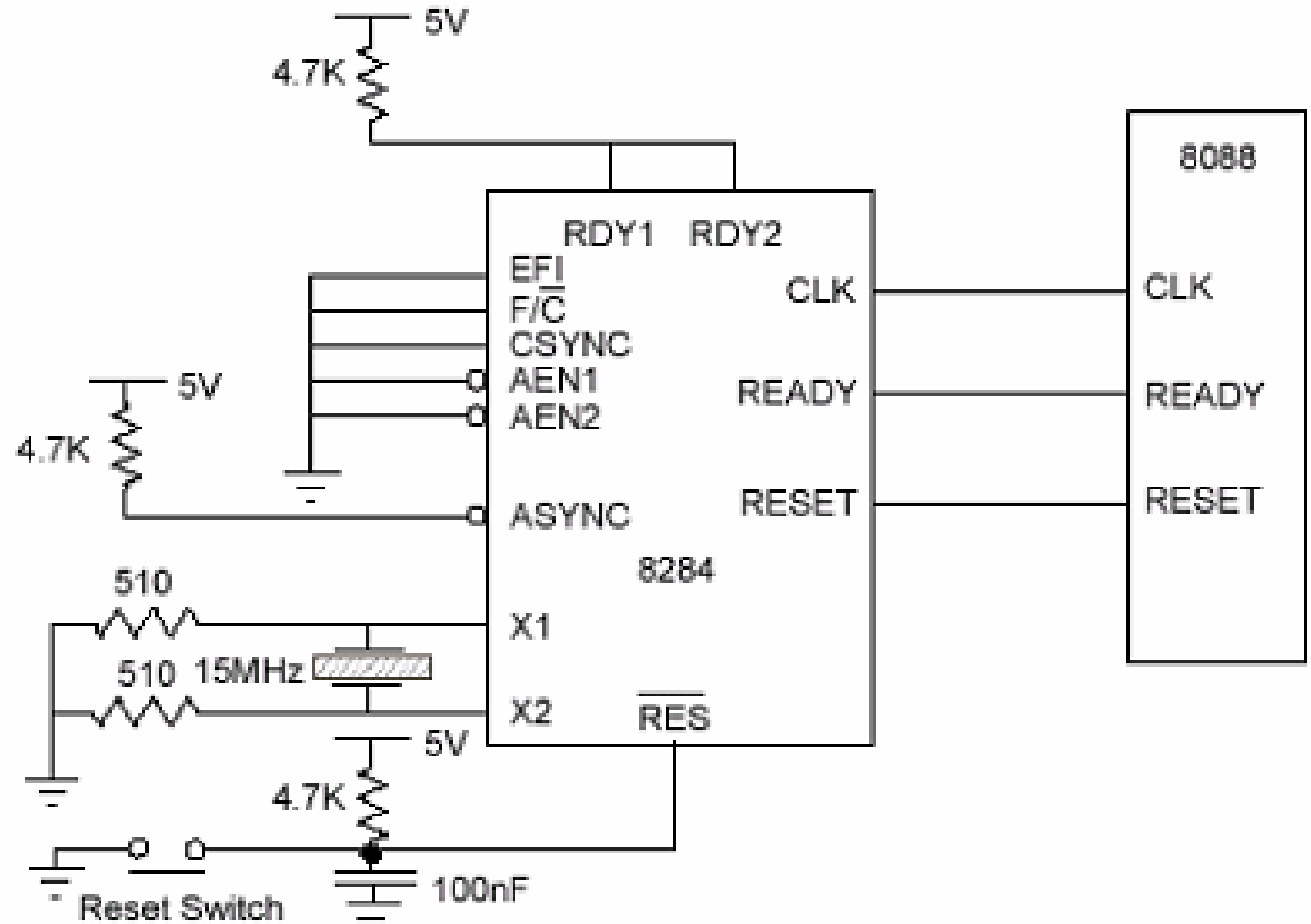
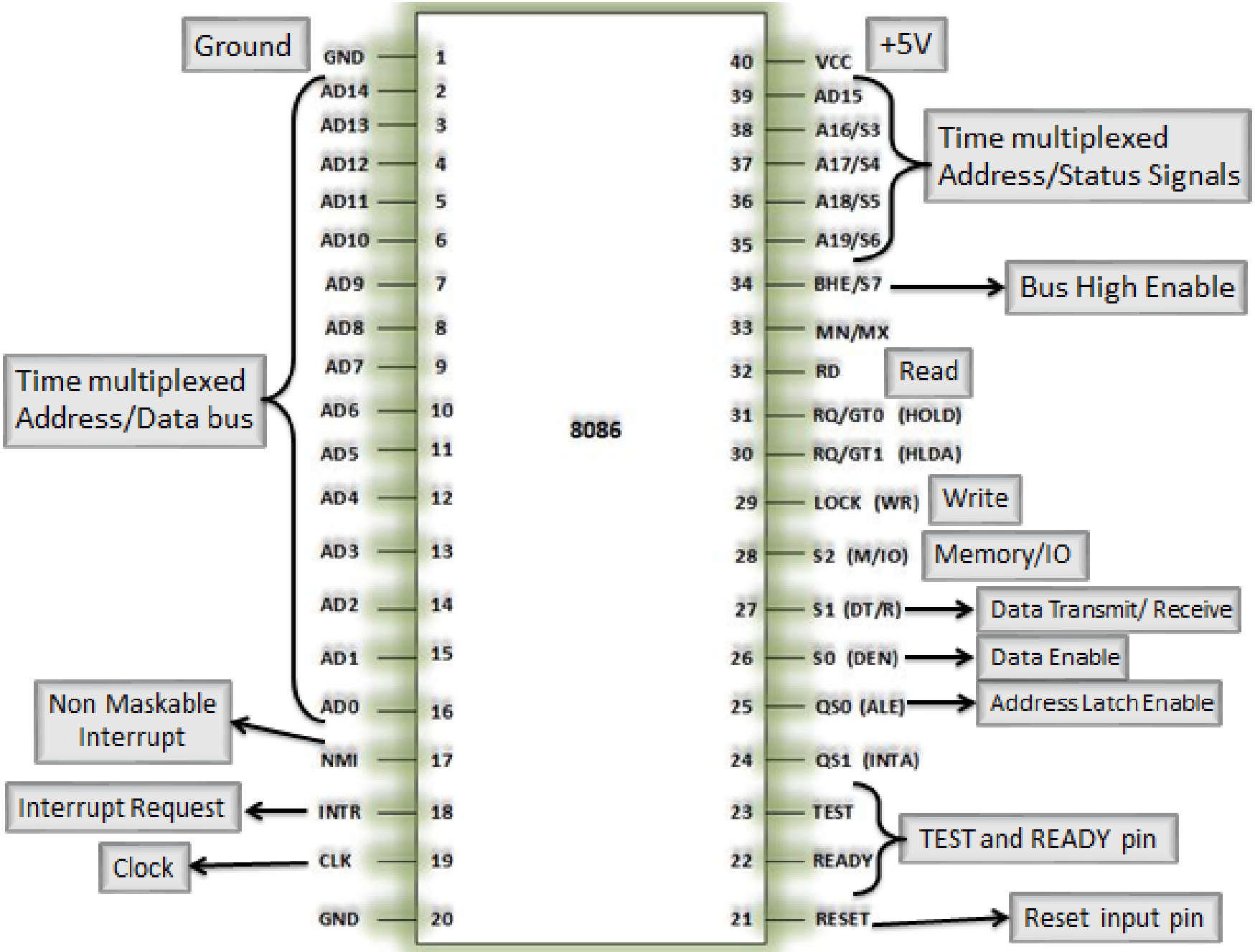
22 READY
21 RESET
+5V
Time multiplexed Address/Status Signals
Bus High Enable
Read
Write
Memory/IO
TEST and READY pin
Reset input pin
Time multiplexed Address/Data bus
Non Maskable Interrupt
Interrupt Request
Clock

Pin Diagram of 8086

CLOCK (heart beat of CPU)

- Clock provides the basic timing for the processor and bus controller.
- It is asymmetric with 33 percent duty cycle to provide optimized internal timing
- Minimum frequency of 5 MHz is required
- 8284 clock generator chip must be connected to the 8086 clock pin, since it does not have on chip clock generator
- The crystal connected to 8284 must have a frequency 3 times the 8086 internal frequency


5V
4.7K
8088
RDY1
RDY2
EFI
F/C
CSYNC
AEN1
AEN2
ASYNC
CLK
READY
RESET
8284
X1
X2
RES
CLK
READY
RESET
510
510
15MHz
5V
4.7K
5V
4.7K
Reset Switch
100nF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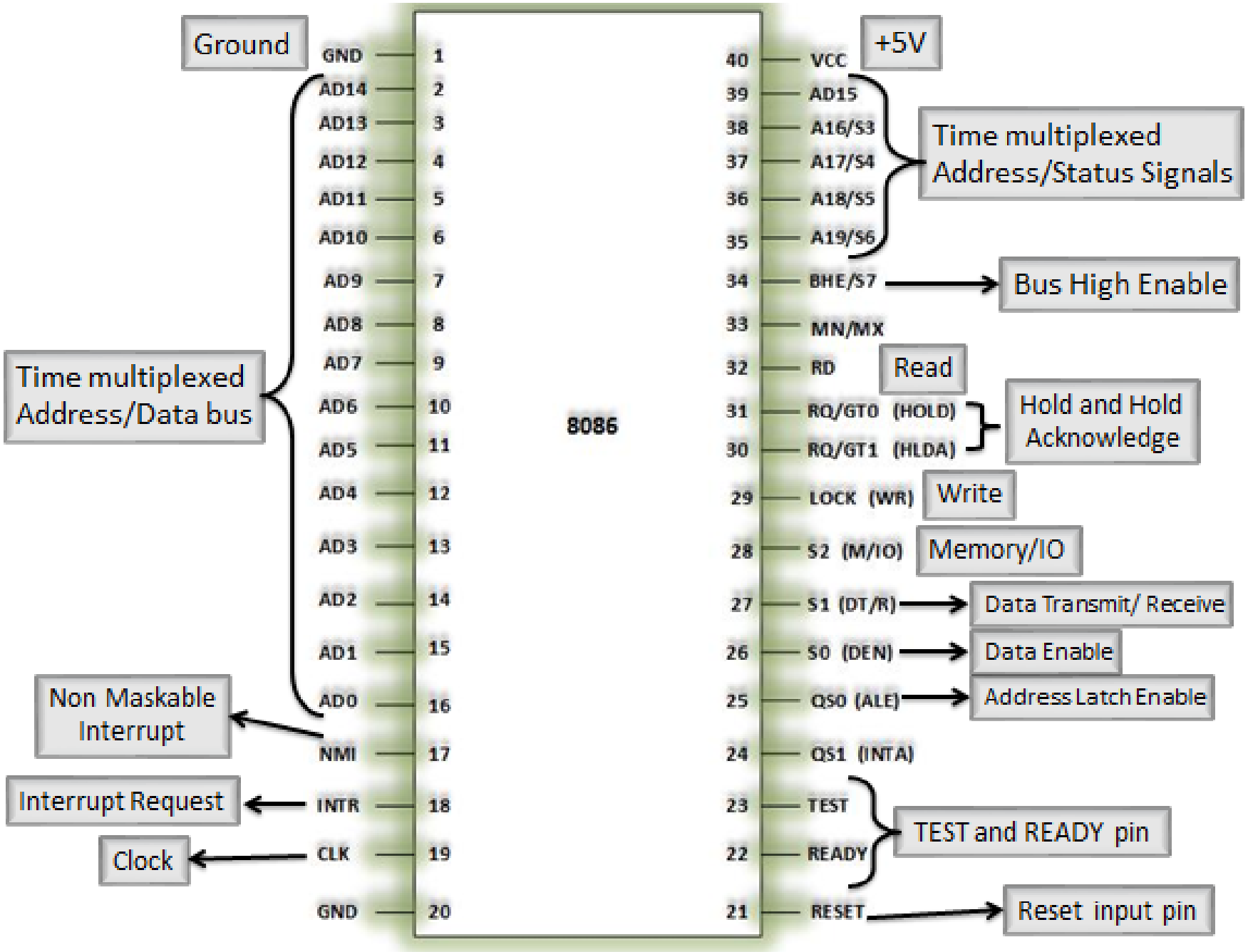
23 TEST
22 READY
21 RESET
8086
+5V
Time multiplexed Address/Status Signals
Bus High Enable
Read
Write
Memory/IO
Data Transmit/ Receive
Data Enable
Address Latch Enable
TEST and READY pin
Reset input pin
Time multiplexed Address/Data bus
Non Maskable Interrupt
Interrupt Request
Clock

Pin Diagram of 8086

ALE : Address Latch Enable
ALE is provided by the processor to latch the address into the 8282/8283 address latch. It is an active high pulse during T1 of any bus cycle.

DT/ R: DATA Transmit/Receive
In minimum mode, 8286/8287 transceiver is used for the data bus. DT/ R is used to control the direction of data flow through the transceiver.

DEN : Data Enable
It is provided as an output enable for the 8286/8287 in a minimum system which uses the transceiver


Ground
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AD11 5
AD10 6
AD9 7
AD8 8
AD7 9
AD6 10
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AD4 12
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AD2 14
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AD0 16
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CLK 19
GND 20
Time multiplexed Address/Data bus
Non Maskable Interrupt
Interrupt Request
Clock
8086
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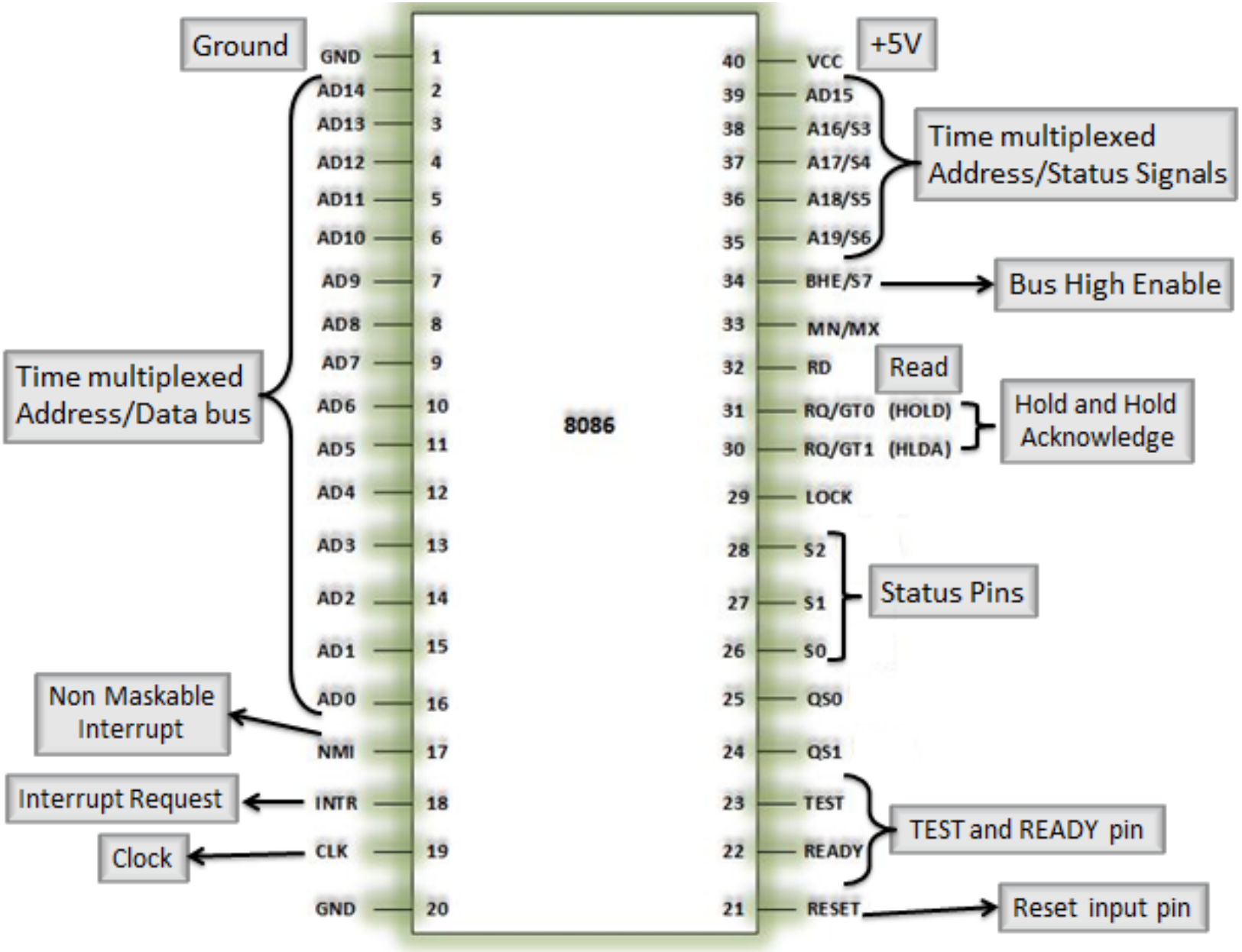
21 RESET
+5V
Time multiplexed Address/Status Signals
Bus High Enable
Read
Hold and Hold Acknowledge
Write
Memory/IO
Data Transmit/ Receive
Data Enable
Address Latch Enable
TEST and READY pin
Reset input pin

Pin Diagram of 8086

HOLD & HLDA (I/O): Hold and Hold Acknowledge

- Hold indicates that another master is requesting a local bus "HOLD"
- To be acknowledged, HOLD must be active HIGH.
- The processor receiving the "HOLD " request will issue HLDA (HIGH) as an acknowledgement in the middle of the T1-clock cycle.
- With the issue of HLDA, the processor will float the local bus and control lines

Pins Specific to Maximum mode only



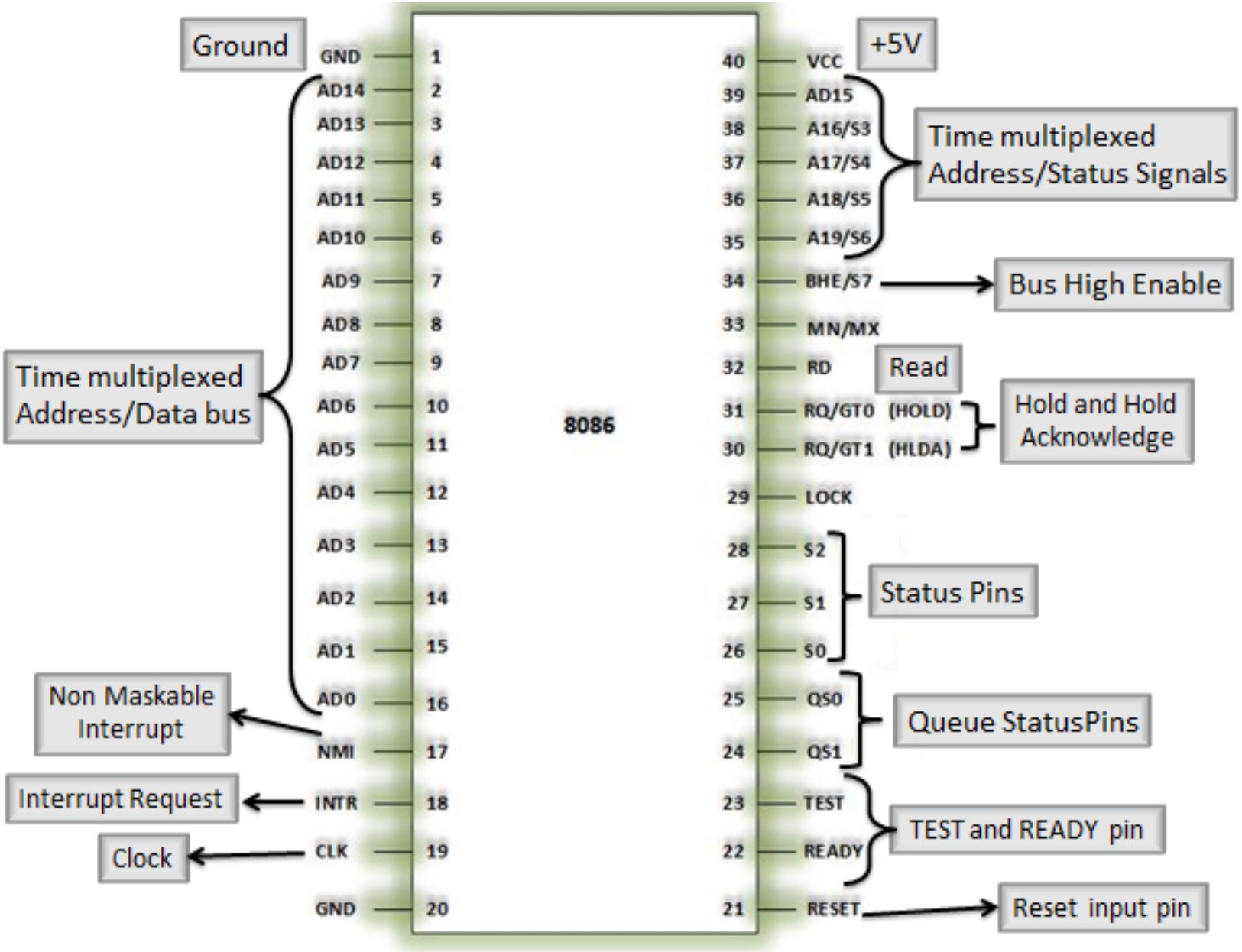
Pin Diagram of 8086

S2, S1, S0 : Status Pins

- These pins are active during T4, T1 and T2 states and is returned to passive state 1,1,1 during T3
- Are used by the 8288 bus controller to generate all memory and I/O operation access control signals

S2	S1	S0	Characteristics
0	0	0	Interrupt acknowledge
0	0	1	Read I/O port
0	1	0	Write I/O port
0	1	1	Halt
1	0	0	Code access1 0 1 Read memory
1	1	0	Write memory
1	1	1	Passive State

Pins Specific to Maximum mode only



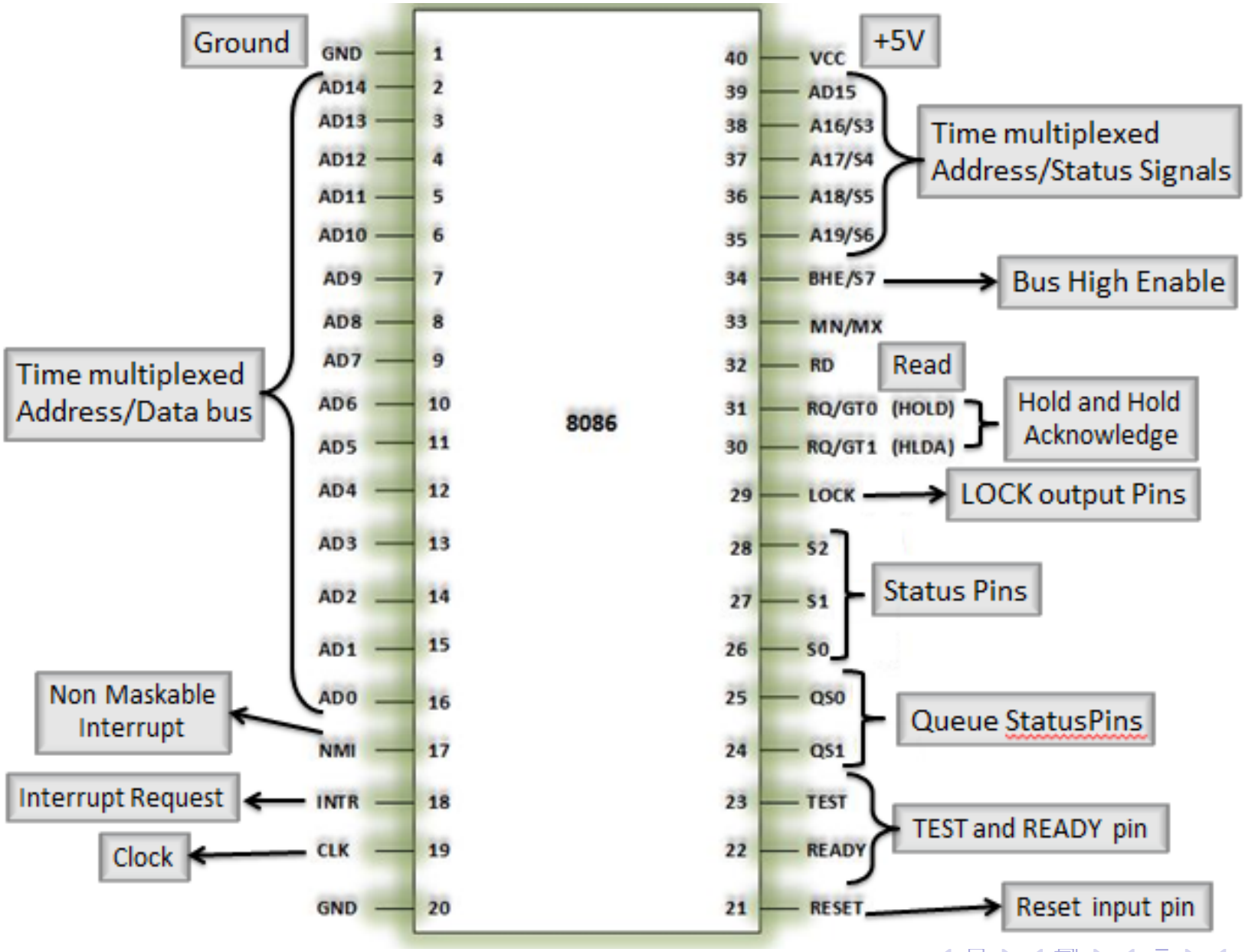
Pin Diagram of 8086

QS0, QS1: Queue Status

- Queue Status is valid during the clock cycle after which the queue operation is performed
- QS0, QS1 provide status to allow external tracking of the internal 8086 instruction queue

QS1	QS1	Characteristics
0	0	No operation
0	1	First byte of opcode from queue
1	0	Empty the queue
1	1	Subsequent byte from queue

Pins Specific to Maximum mode only

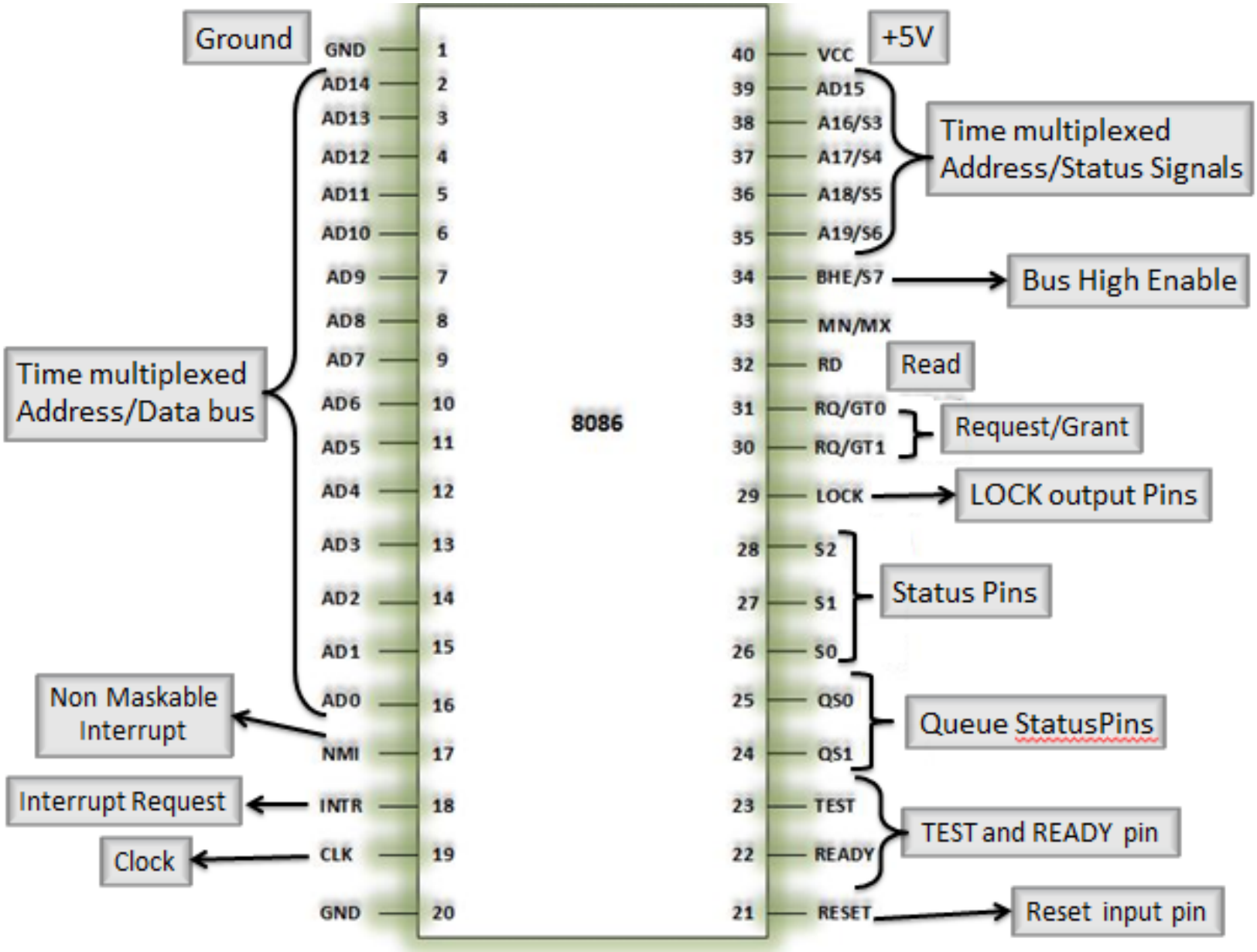


Pin Diagram of 8086

LOCK

- It indicates to another system bus master, not to gain control of the system bus while LOCK is active Low
- The LOCK signal is activated by the "LOCK" prefix instruction and remains active until the completion of the instruction
- This signal is active Low and floats to tri-state OFF during 'hold acknowledge'

Pins Specific to Maximum mode only



Pin Diagram of 8086

RQ/GT0 and RQ/GT1 (I/O): Request/Grant

- Are used by other processors in a multi processor organization
- Local bus masters of other processors force the processor to release the local bus at the end of the processors current bus cycle
- Each pin is bi-directional and has an internal pull up resistors. Hence they may be left un-connected

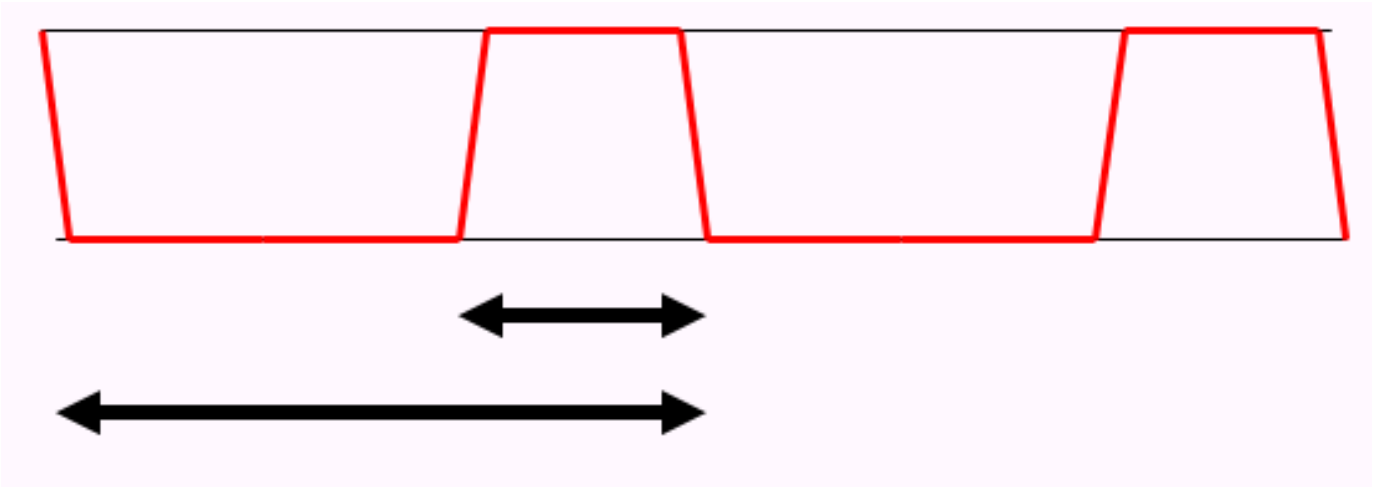
8284 CLOCK GENERATOR

- Ancillary component to the 8086/8088 microprocessors
- The 8284 provides the following basic functions or signals:
  - Clock generation (CLK)
  - RESET synchronization
  - READY synchronization
  - TTL level peripheral clock (PCLK)

8284 CLOCK GENERATOR

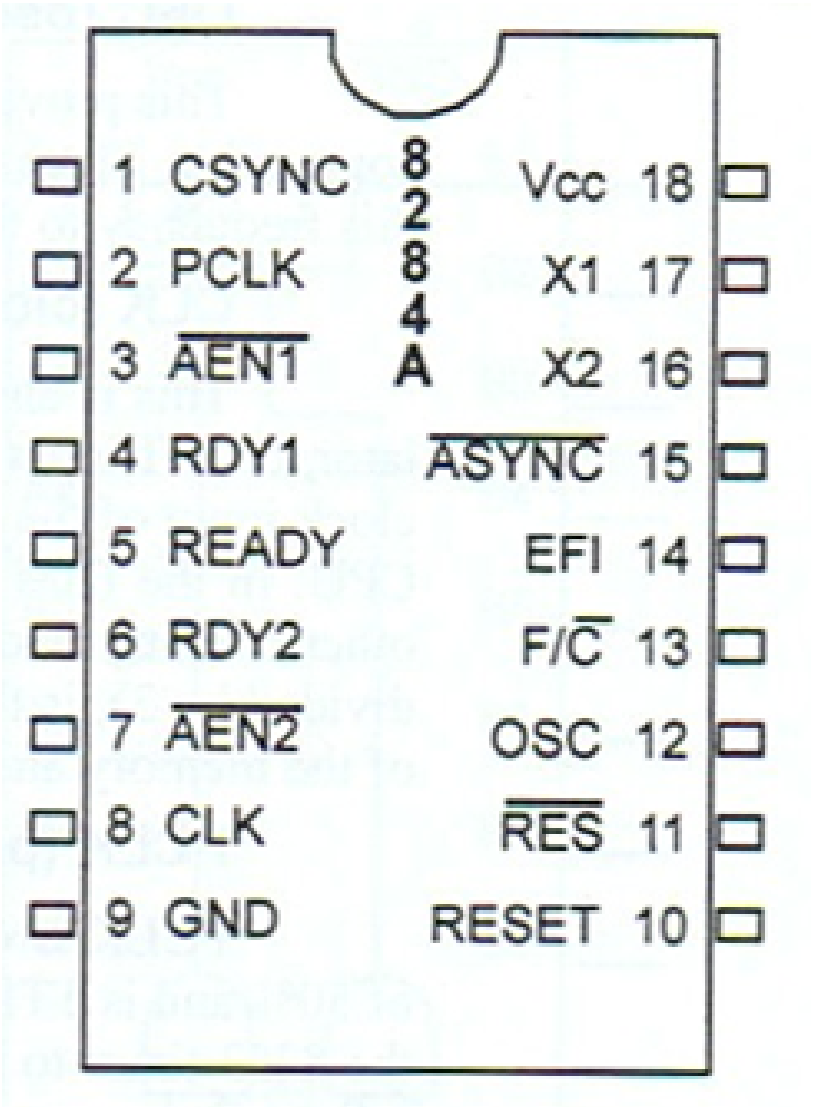
The 8088/8086 require a specific waveform for the system clock

- Fast rise and fall times (¡10ns)
- Logic 0: -0.5 to 0.6 V
- Logic 1: 3.9 to 5.0 V
- Duty cycle of 33



33% duty cycle

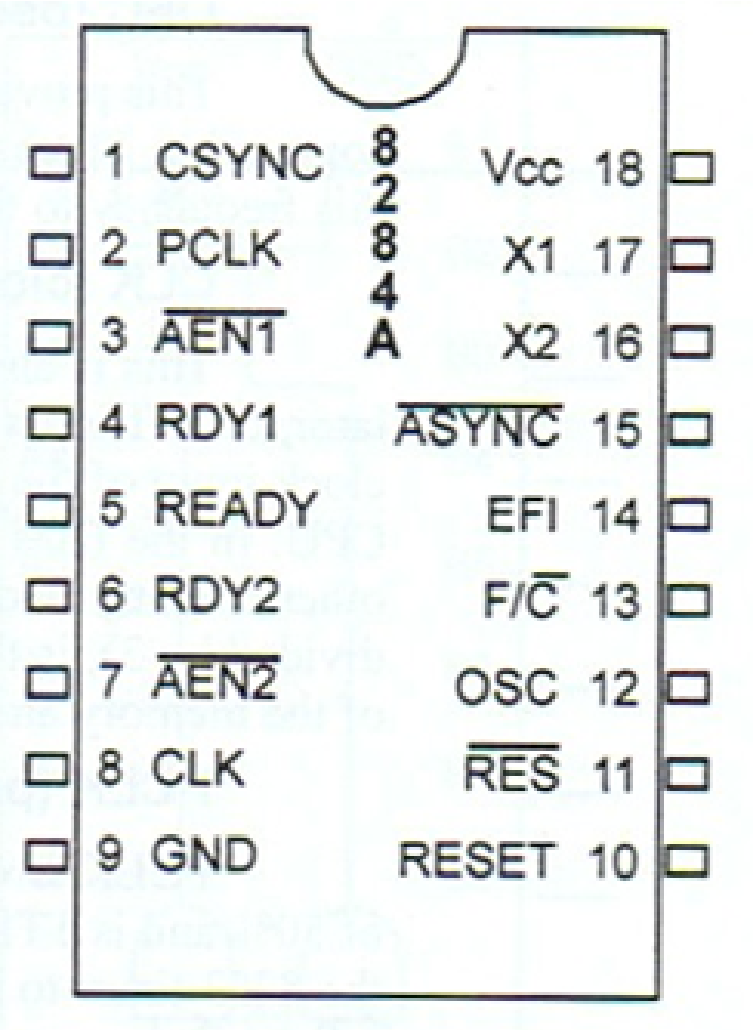
8284 CLOCK GENERATOR



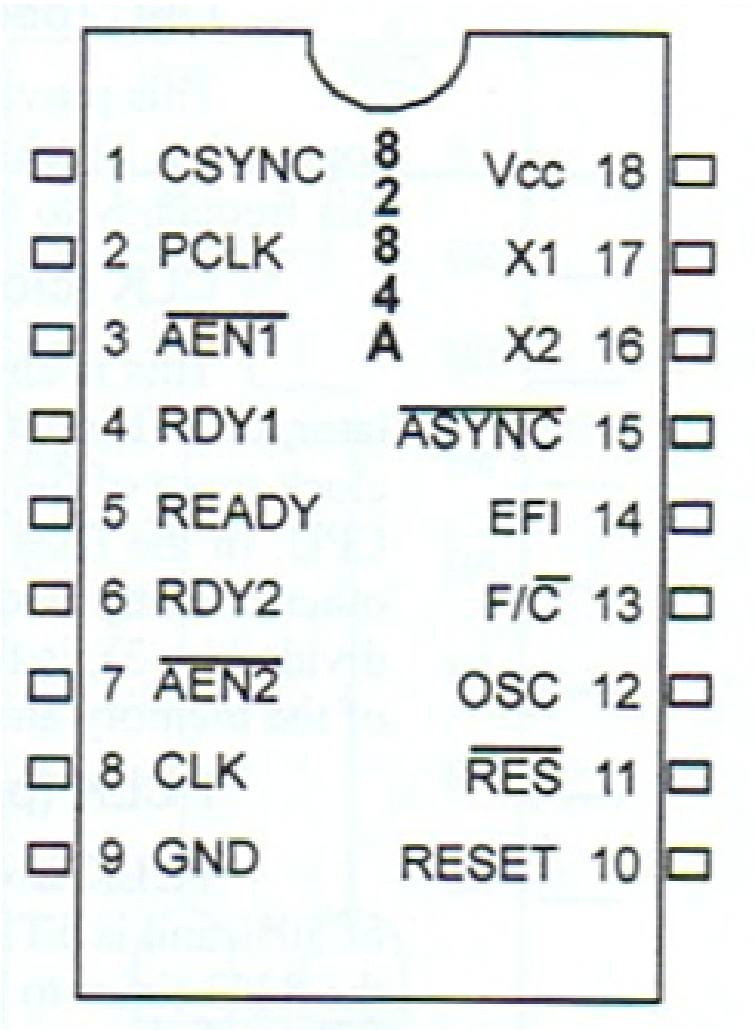
8284 CLOCK GENERATOR

Input Pins

- RES (Reset In): from power supplier
- X1 and X2 (Crystal In): the crystal frequency must be 3 times the desired frequency for the microprocessor
- RDY1 and AEN1: provide a Ready signal to processor, which will insert a WAIT state to the CPU read/write cycle
- RDY2 and AEN2: For multiprocessor systems



8284 CLOCK GENERATOR



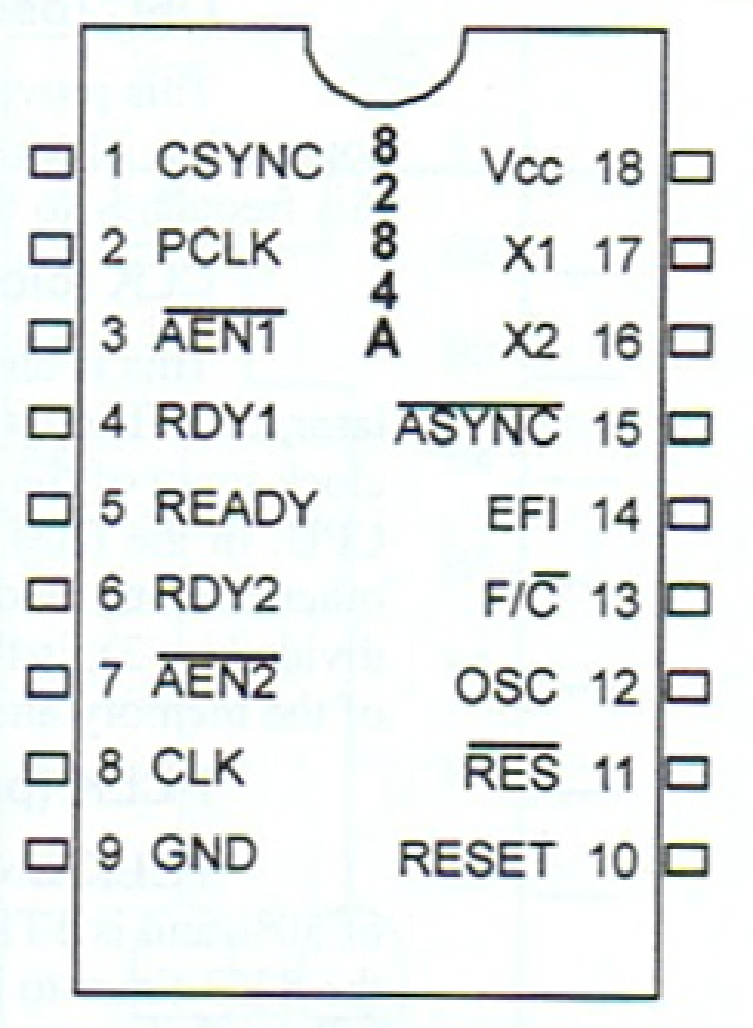
Output Pins

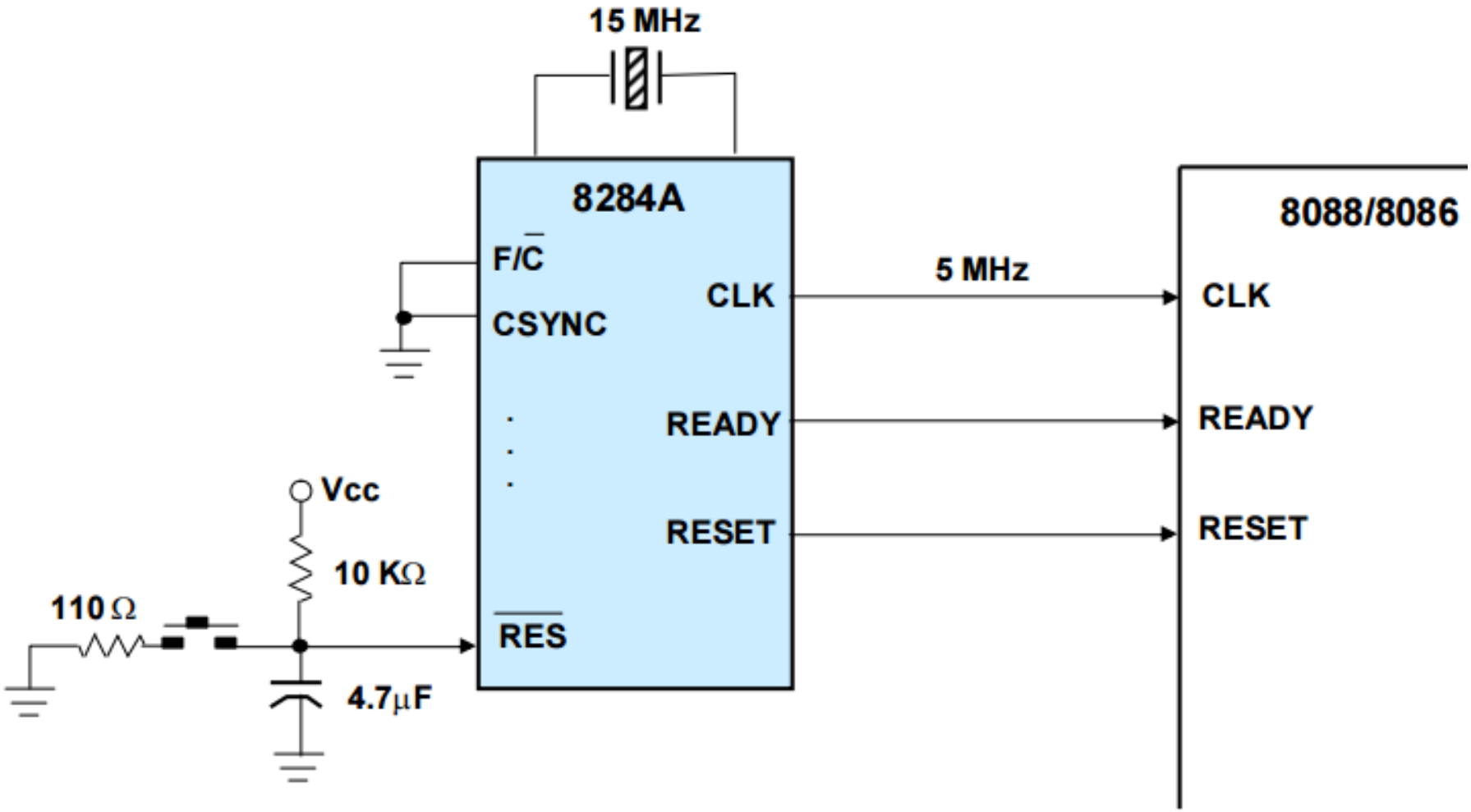
- RESET: reset signal to the 8086/88, activated by RES
- OSC (oscillator):
  provide to the expansion slot
- CLK (clock):
  1/3 of the crystal input,
  with a duty cycle of 33%
- PCLK: one-half of CLK (1/6 of crystal) with duty cycle of 50% and is TTL compatible.
- READY:
  connect to READY input
  of CPU to insert WAIT state

8284 CLOCK GENERATOR

Output Pins

- F/C (Frequency/crystal select): If 1, an external clock is provided to the EFI input pin and if 0, an external crystal oscillator connected to X1 and X2 provides the clock
- EFI (External frequency Input): Supplies the timing whenever the F/C is high.
- CSYNC (Clock Synchronization): Used whenever the EFI input provides synchronization in systems with multiple processors. If the internal crystal oscillator is used,




15 MHz
8284A
F/C
CSYNC
CLK
READY
RESET
RES
5 MHz
8088/8086
CLK
READY
RESET
Vcc
10 KΩ
110 Ω
4.7μF

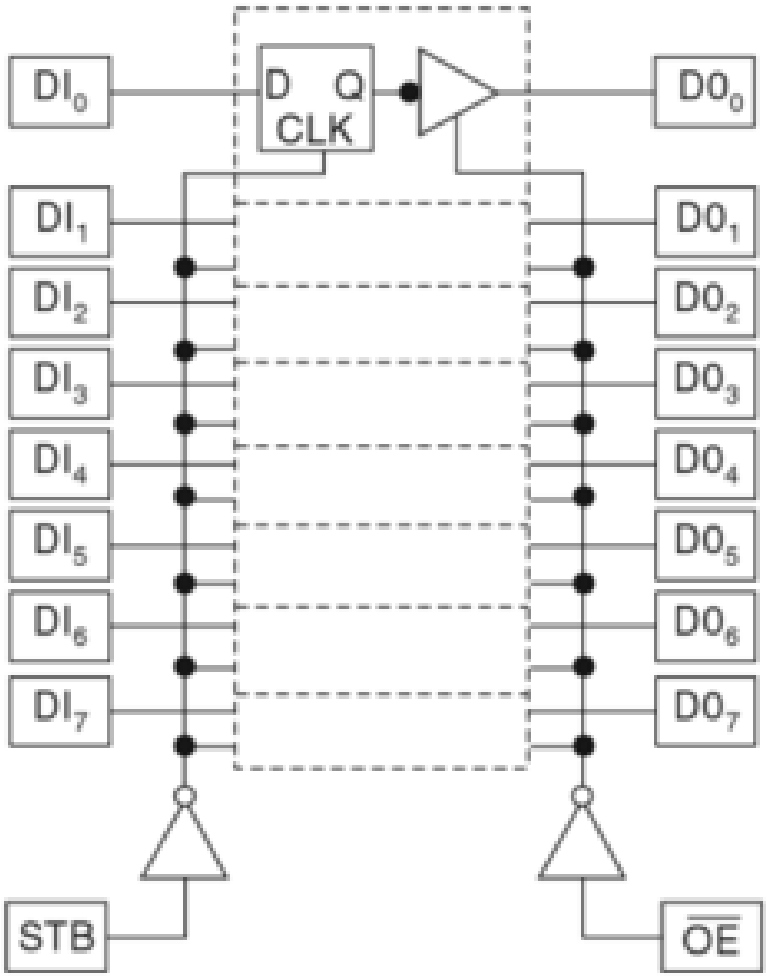
8282/8283 LATCH

8282/8283 LATCH

- CMOS octal latching buffer
- provides an eight bit parallel latch/buffer in a 20 pin package
- Basically de-multiplexing the data and addressing bus
- OE (Output Enable) connected to GND, the chip is selected
- STB (Strobe) is connected to the pin ALE (Address Latch Enable) of the processor and takes over the address data from the multiplexed address-/databus

Latches are used to de-multiplex the address/data and address/status lines and commonly have output buffers for driving external loads.

8282 LATCH



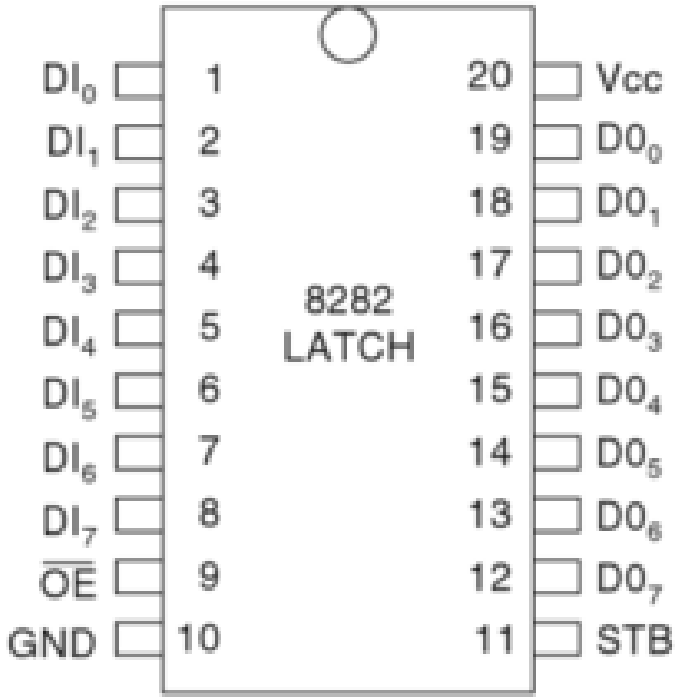
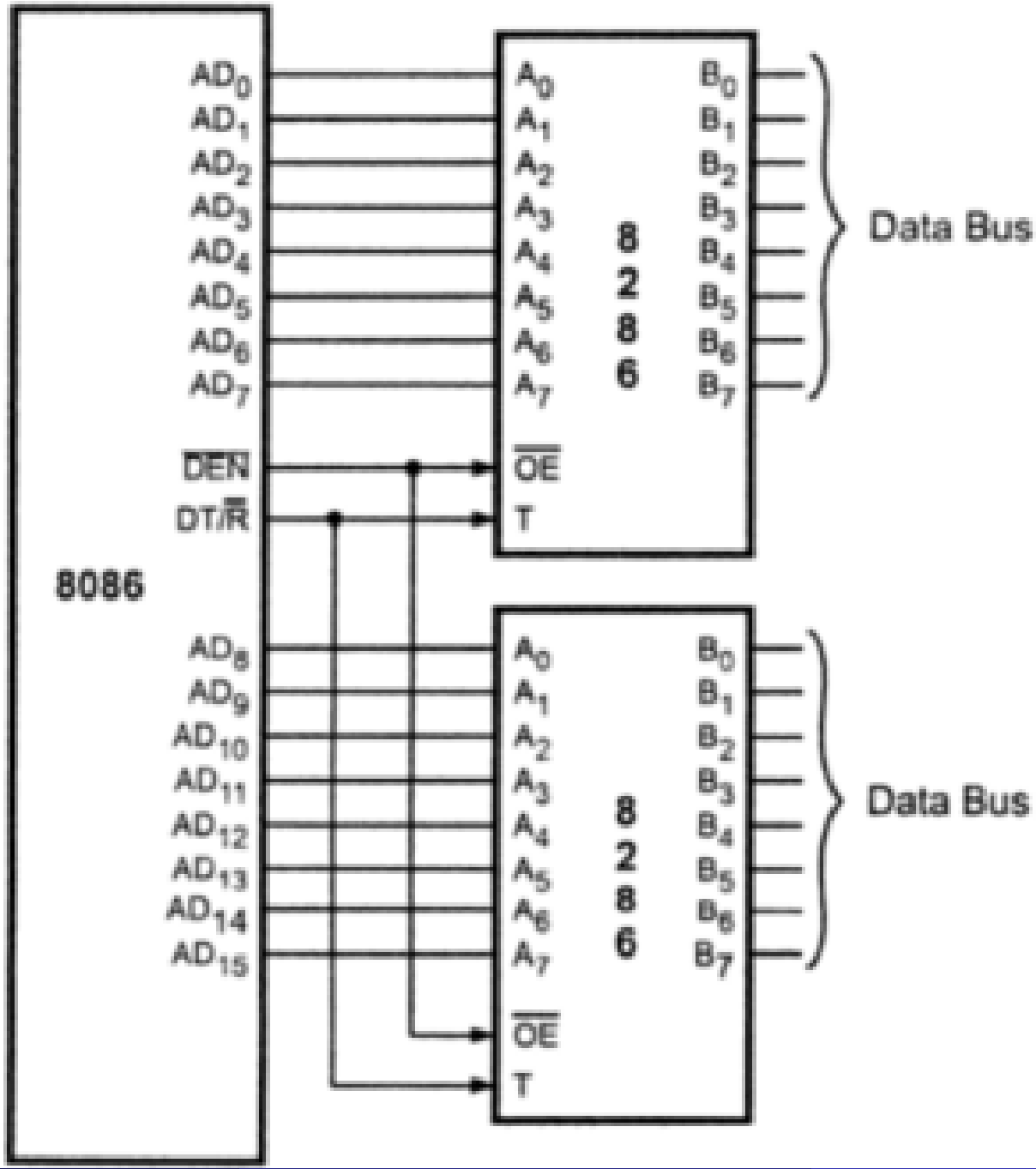


Figure: Functional Diagram and Pin Diagram

8286 TRANSCEIVER

8286 TRANSCEIVER

- If a system includes several interfaces then to increase current sourcing/sinking capacities it is necessary to use drivers and receivers for data bus also
- Intel 8286 device is used to implement the transceiver block


8086
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
DEN
DT/R
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
A0
A1
A2
A3
A4
A5
A6
A7
OE
T
8286
B0
B1
B2
B3
B4
B5
B6
B7
Data Bus
Data Bus

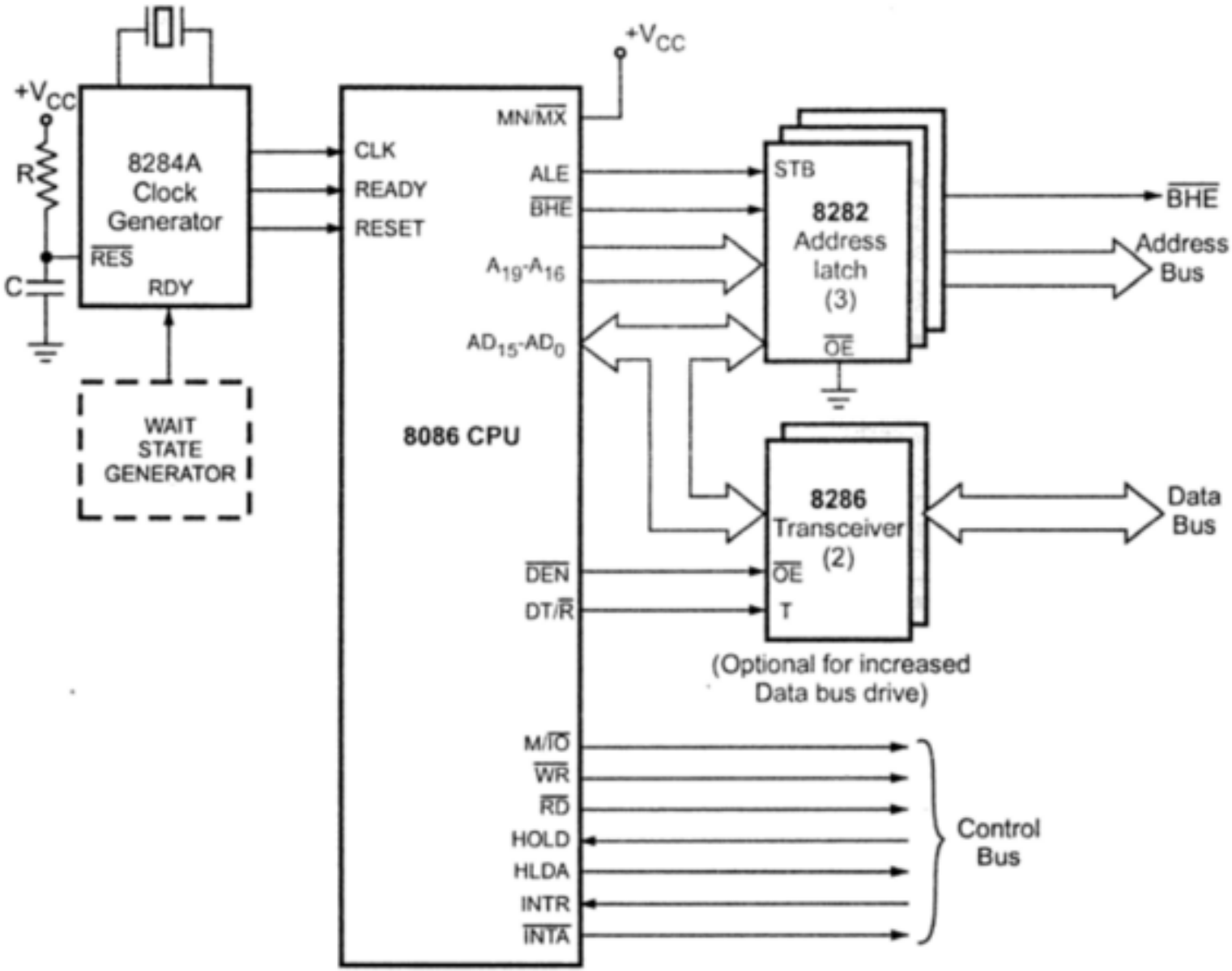
8286 TRANSCEIVER

- If a system includes several interfaces then to increase current sourcing/sinking capacities it is necessary to use drivers and receivers for data bus also
- Intel 8286 device is used to implement the transceiver block
- It has 16- tri state elements, 8 receivers and 8 drivers
- That's why TWO 8286 are required to service 16 data lines of 8086
- DT/R is connected to T input, which controls the direction of data flow

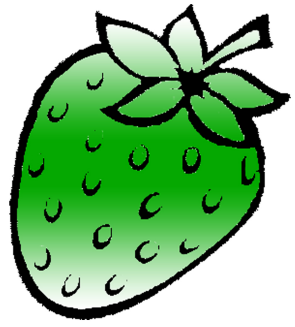
8286 TRANSCEIVER

- DT/$\overline{R}$ is connected to T input, which controls the direction of data flow
  - When this signal is low, receivers are enabled, so that 8086 can read data from memory and I/O device
  - When this signal goes high, drivers are enabled allowing 8086 to transfer(or write) data into memory and I/O device
- To enable output of transceiver its $\overline{OE}$ pin should be low, That's why it is connected to DEN pin of 8086.
  - Since $\overline{DEN}$ signal goes low when CPU is ready to send or receive data

Basic Minimum mode configuration



STRAWBERRY



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