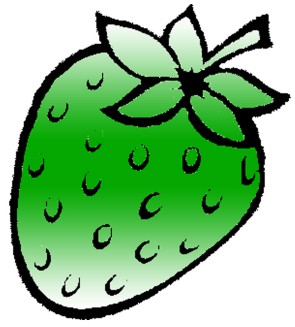
STRAWBERRY



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INTERFACING

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February 29, 2016

DMA ; Direct Memory Access Controller (8257)

Introduction

Can I/O have direct access to memory?

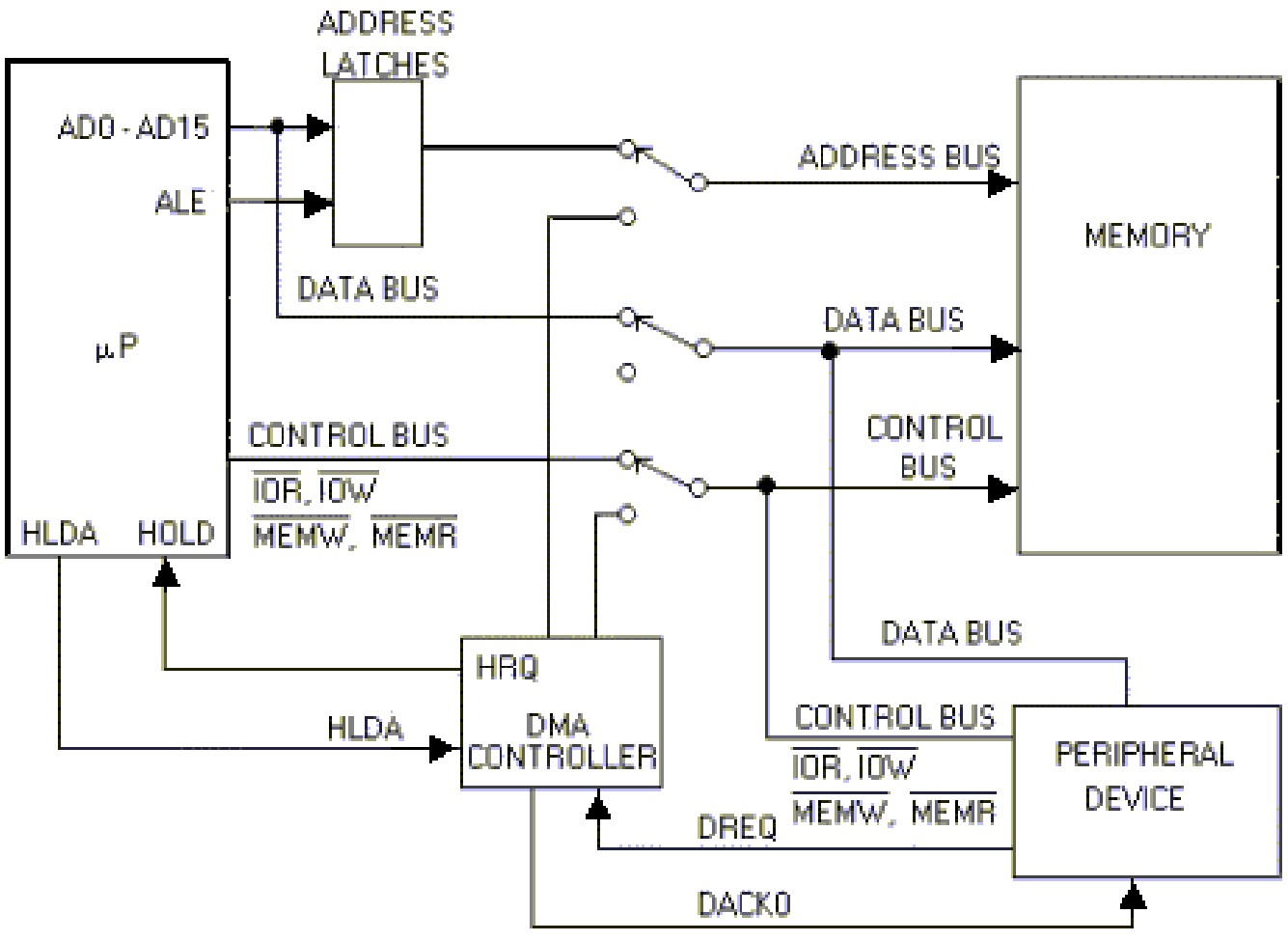
Introduction

Can I/O have direct access to memory?

Yes, But under supervision

The device which supervises data transfer is named as DMA controller.

DMA operation in general



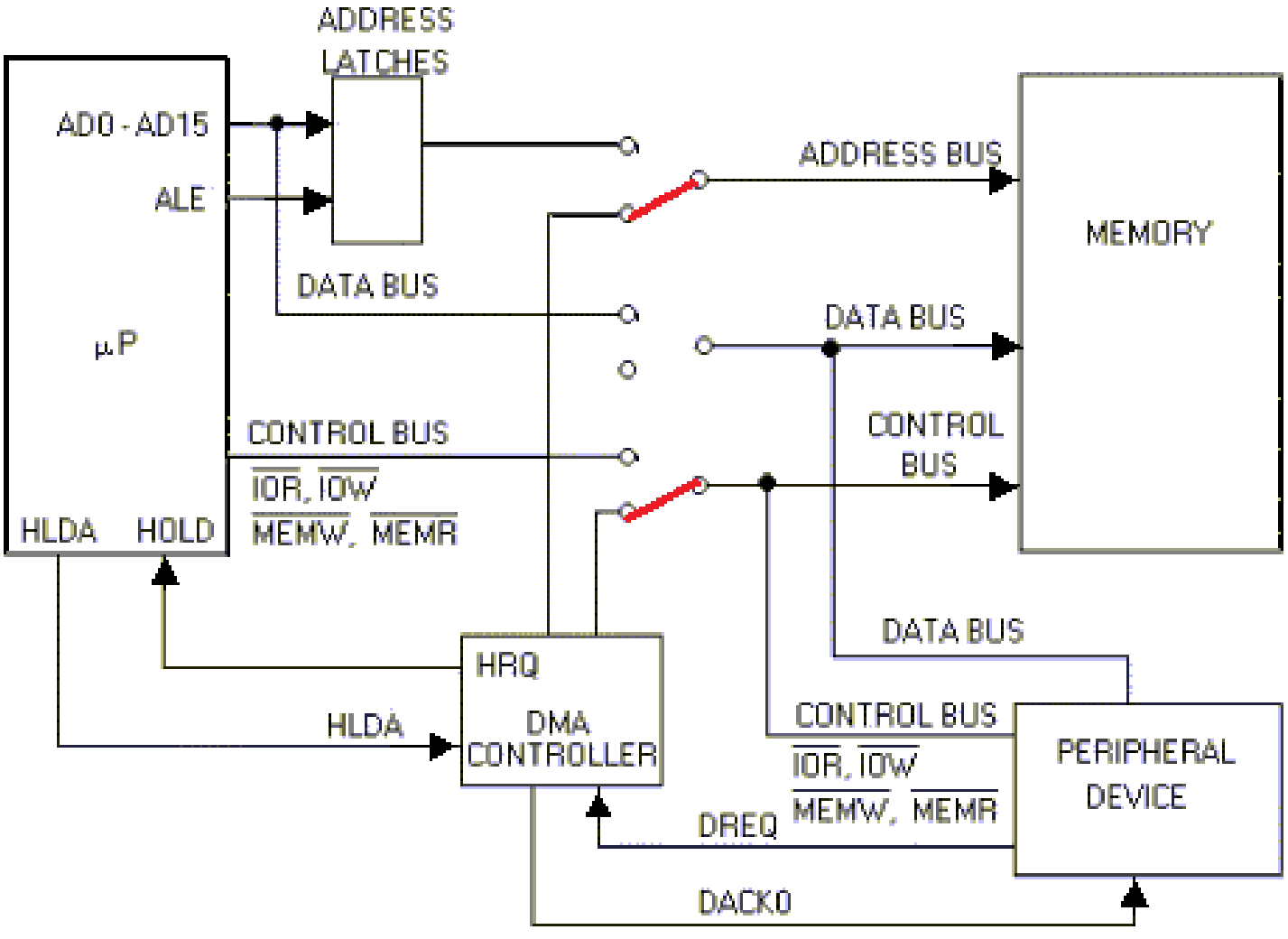
DMA operation

when memory are connected to CPU:

- No direct access to memory by I/O device
- Processor is master of all three buses: address,data, control
- Processor treats DMA controller as I/O device only , IN and OUT instructions are used

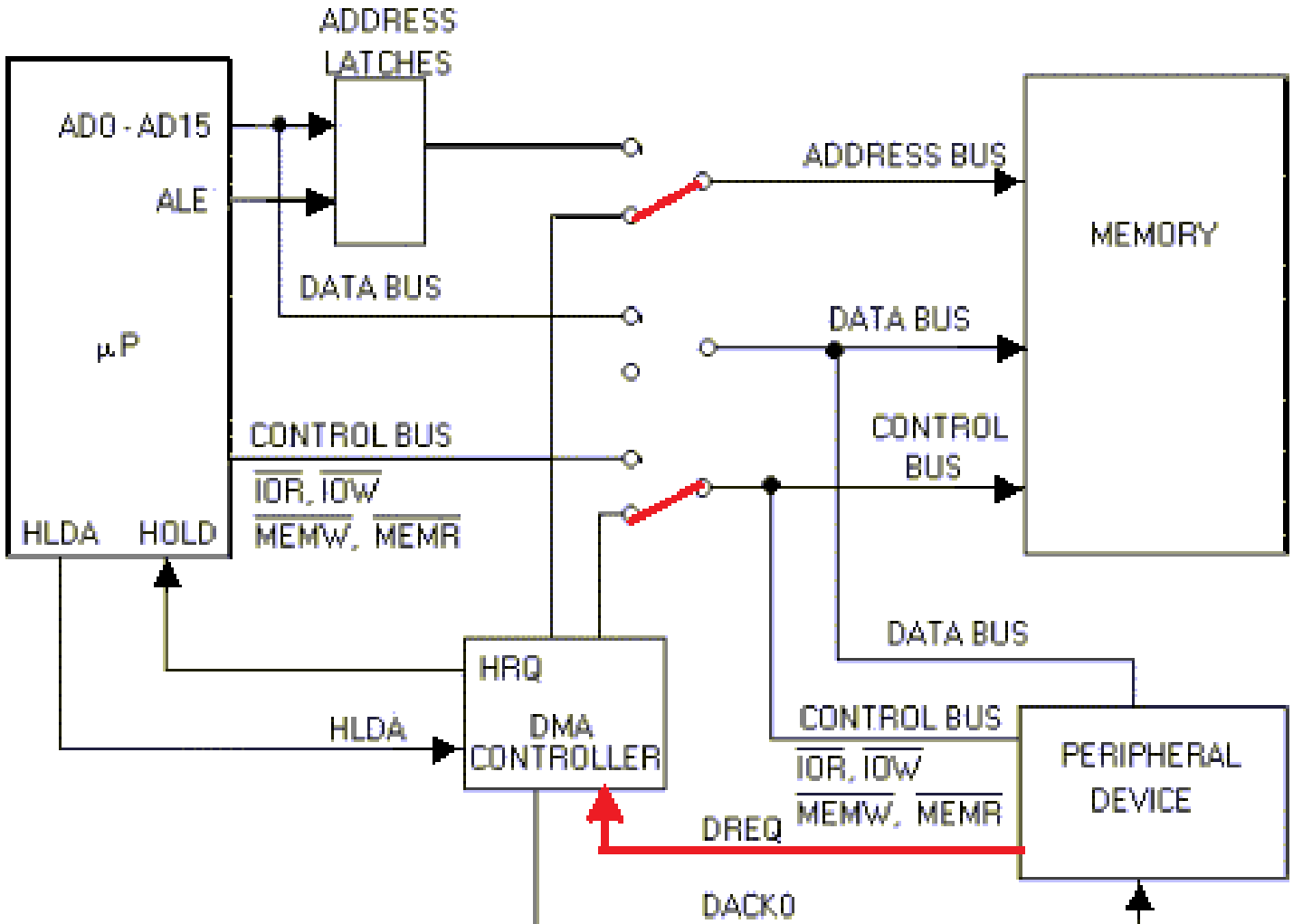
DMA operation

When memory is not connected to CPU, DMA comes in to role



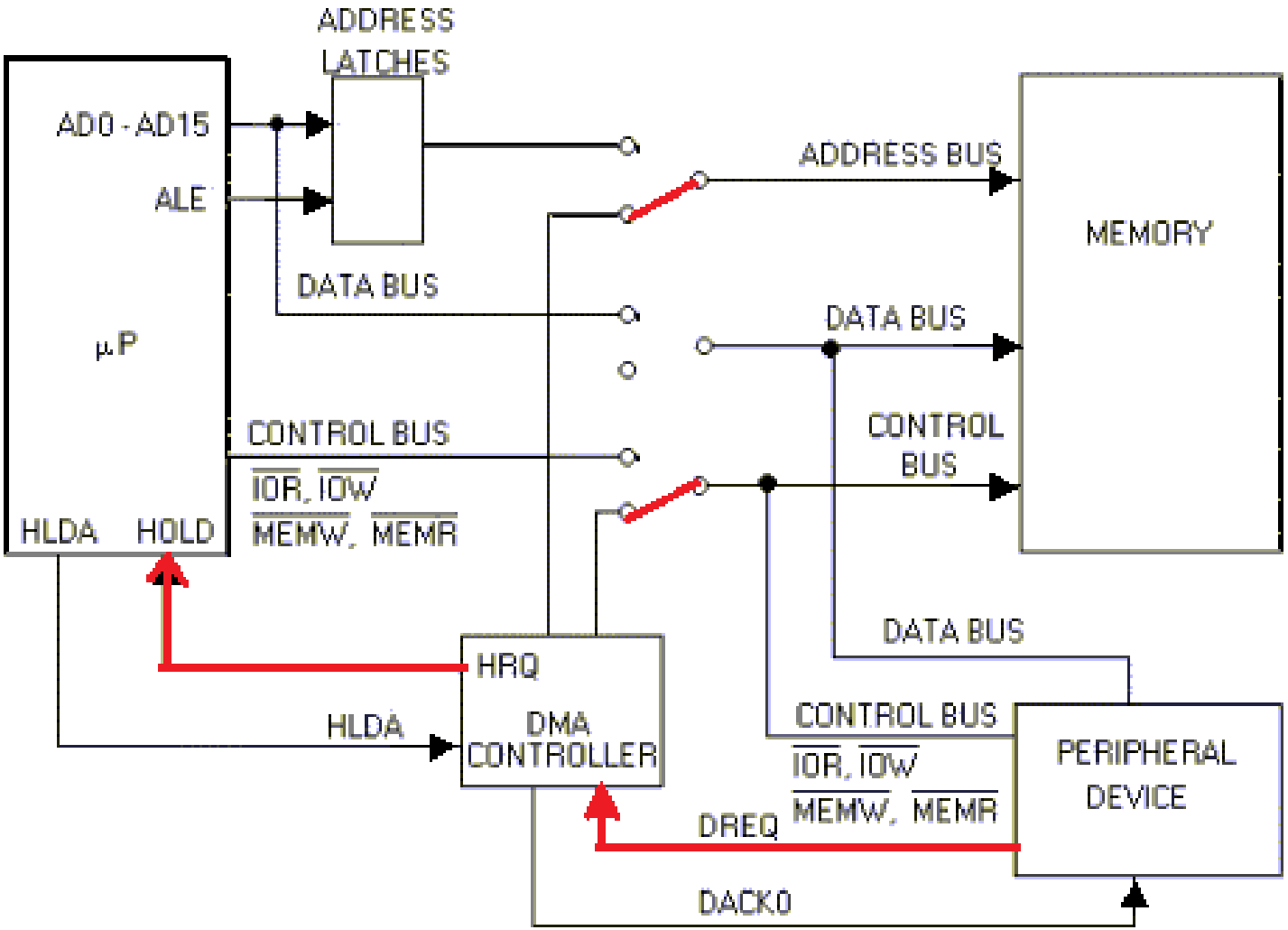
DMA operation

when Peripheral device is ready to access memory directly it generates a request



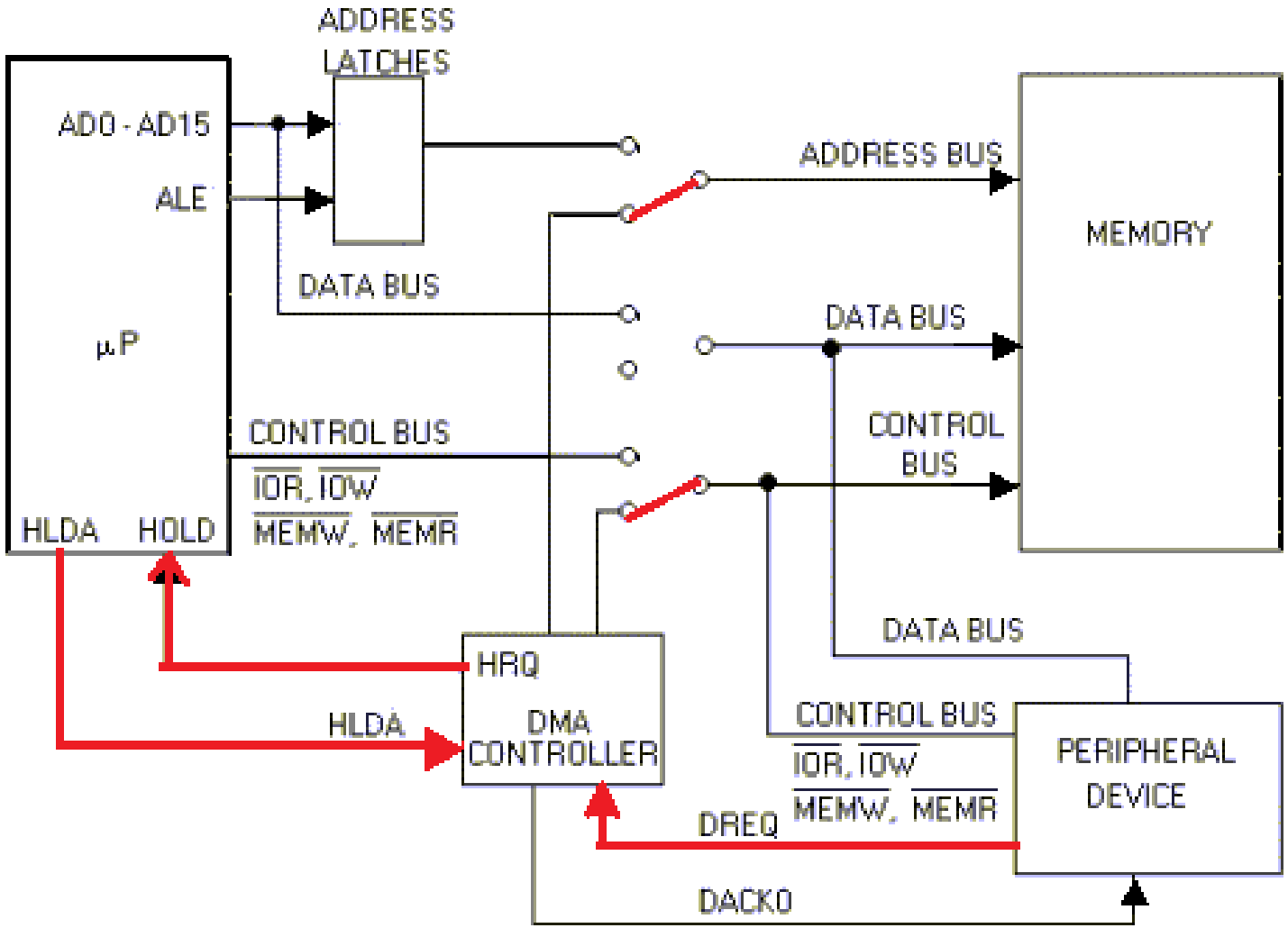
DMA operation

DMA controller activates HOLD requests, asking controller to hold for some time and make him the master of all the three buses.



DMA operation

Microprocessor will complete the on going task and send a hold acknowledge

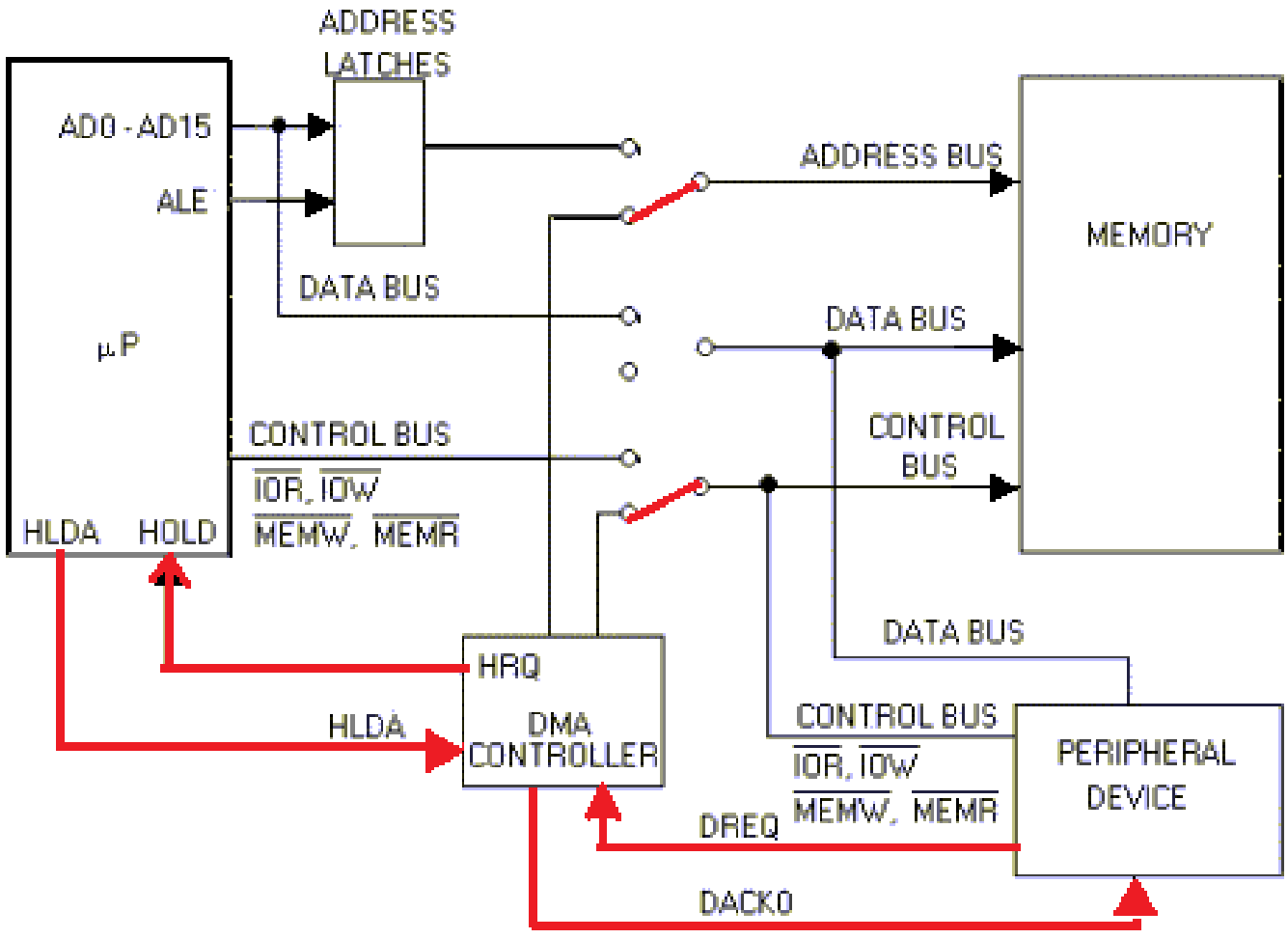


DMA operation

The microprocessor tristates all its buses, so total cut off from memory and I/O device.
DMA controller becomes the master

DMA operation

DMA controller sends an acknowledge to the peripheral device, informing it that direct access is allowed



DMA operation

- Data flows from memory to I/O device and vice-versa
- After data transfer, DMA deactivates HOLD line and switch position changes
- Processor regains control

DMA controller: Data Transfer Modes (3- Modes)

BURST or BLOCK TRANSFER DMA:

- Fastest DMA mode
- Two or more data bytes are transferred continuously
- N number of DMA cycles are added to the microprocessor machine cycle, where N is the no. of bytes that are transferred
- After sending one byte, it increments the memory address, decrements counter and transfers the next byte

DMA controller: Data Transfer Modes (3- Modes)

CYCLE STEAL or SINGLE BYTE TRANSFER DMA

- only one byte of data is transferred at a time
- slower than the burst DMA
- one DMA cycle is added between two machine cycles of processor

DMA controller: Data Transfer Modes (3- Modes)

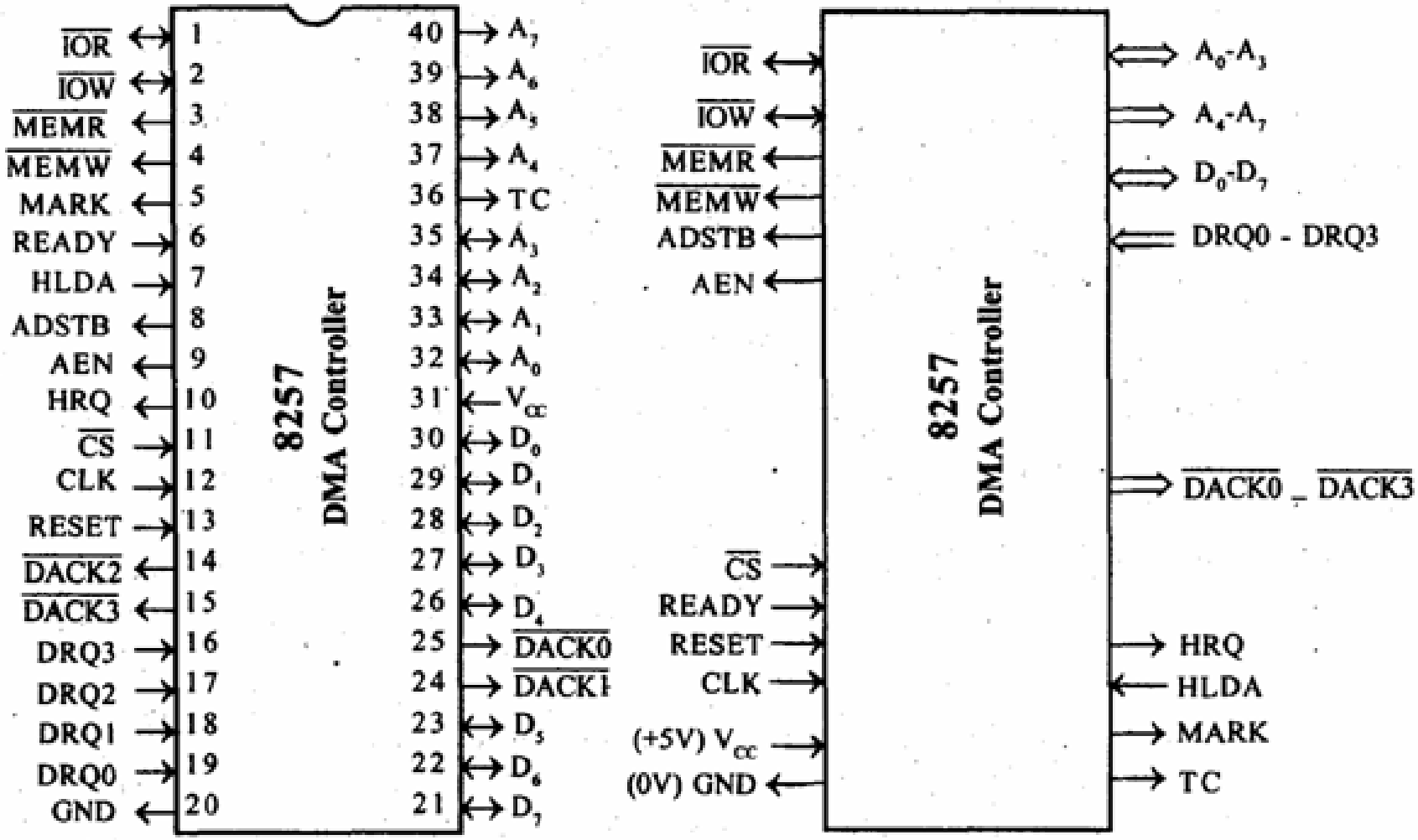
TRANSPARENT or HIDDEN DMA TRANSFER

- slowest transfer
- microprocessor executes some states in which it floats the address and data bus
- microprocessor is isolated
- DMA transfer data during these states, without the knowledge of processor

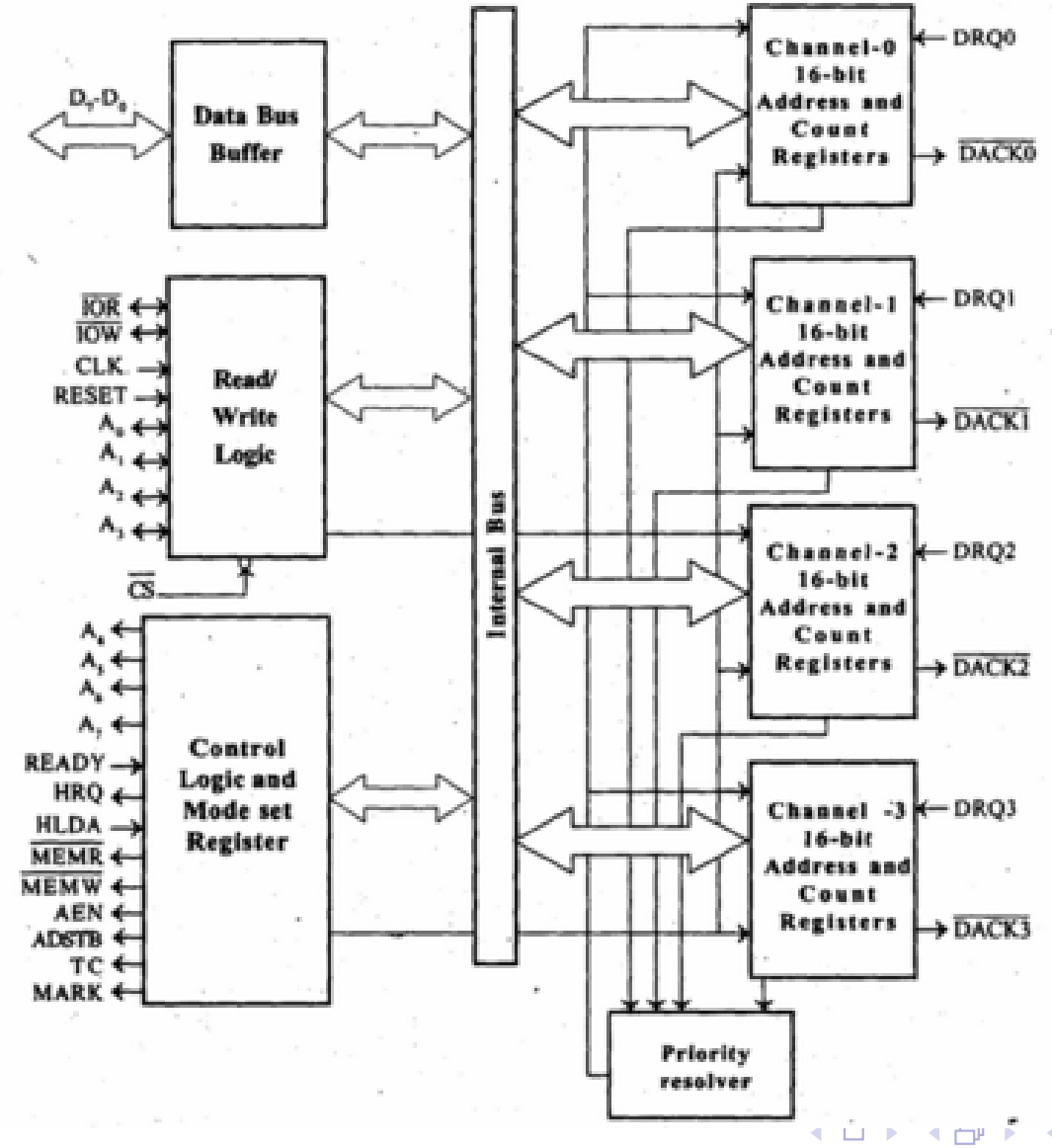
Programmable DMA controller : 8257

- Four channel DMA controller (4 I/O devices can be interfaced)
- On chip priority resolver
- Frequency: 250 KHz - 3 MHz
- used in block or cycle steal transfer
- Executes 3 DMA cycle: DMA read, DMA write and DMA verify
- 16-bit address register and 14 bit counter in every channel

Programmable DMA controller : 8257



Programmable DMA controller : 8257



Programmable DMA controller : 8257

Data Bus Buffer :

- Tristate, bi-directional buffer
- In slave mode; transfers data between microprocessor and internal bus
- Directional of data buffer is set by read/write logic control
- In Master mode; outputs memory address

Programmable DMA controller : 8257

Read/Write Logic Block :

- In slave mode, accepts address bits and controls signals from microprocessor
- In master mode; generates address bits and control signals
- Control all internal read/write operations
- contains F/L Flipflop

Programmable DMA controller : 8257

Read/Write Logic Block :

IOR and IOW : In slave mode both act as input line (by processor to read/write contents of/in 8257 registers) , but in master mode they act as output line.

A0 - A3 : Bidirectional address line. In slave mode, used as address inputs and used to access one of the registers. In master mode; used as address output lines.

Programmable DMA controller : 8257

Control Logic Block :

- Contains control logic, mode set register and status register
- increments 16 bit address and decrements 14 bit count register
- Activates HRQ signal on channel DMA request

Programmable DMA controller : 8257

Control Logic Block :

A4 - A7 : Address output lines. In slave mode they are tristated. In master mode places address of memory.

READY : used to interface slow devices, When READY = 0, DMAC adds wait states.

Programmable DMA controller : 8257

Control Logic Block :

HRQ : Hold request output line

HLDA : HOLD acknowledge input line

MEMR/MEMW : output control signals for memory read and memory write

TC : Terminal count. output status signal activated in master mode only. TC =1 , when content on count register is zero during block transfer.

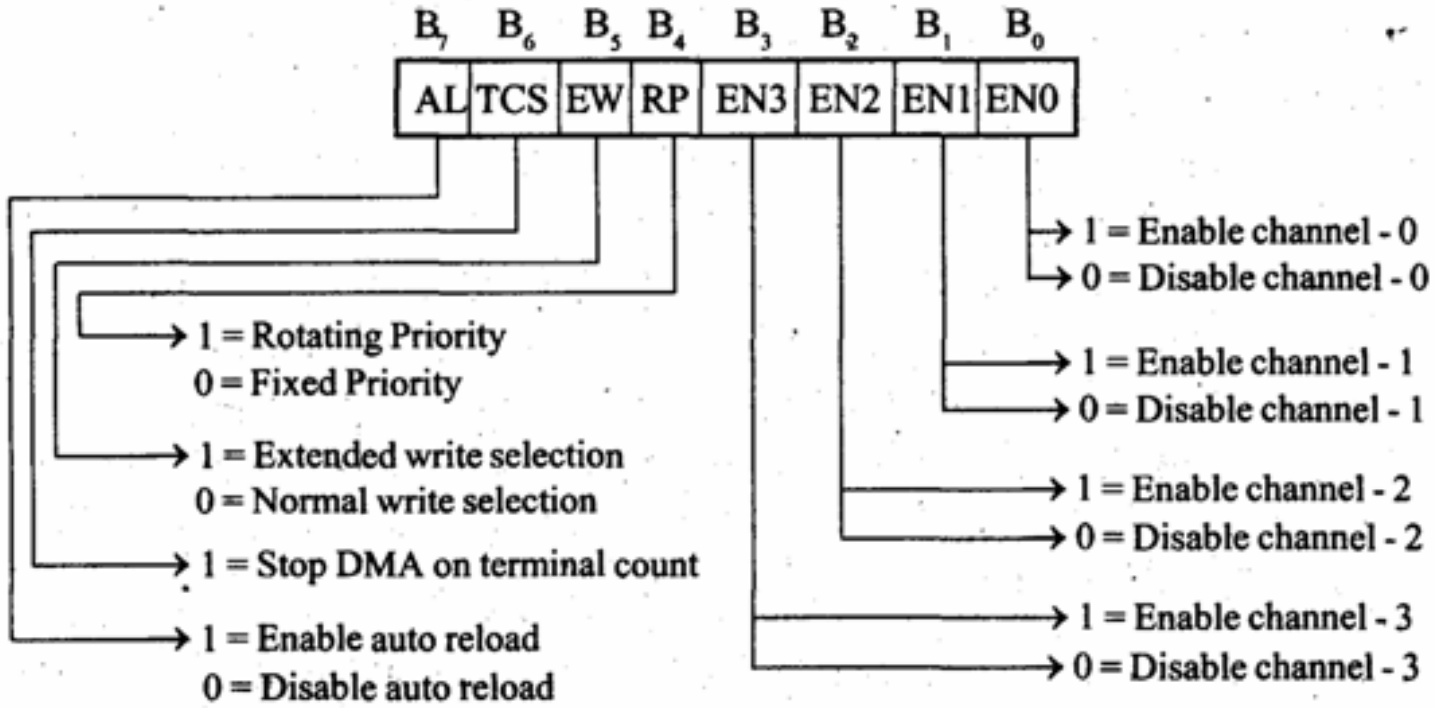
MARK : Output line active during master mode. It goes high after transferring every 128 bytes of data.

Programmable DMA controller : 8257

Control Logic Block :

Mode set register : used to set operating modes

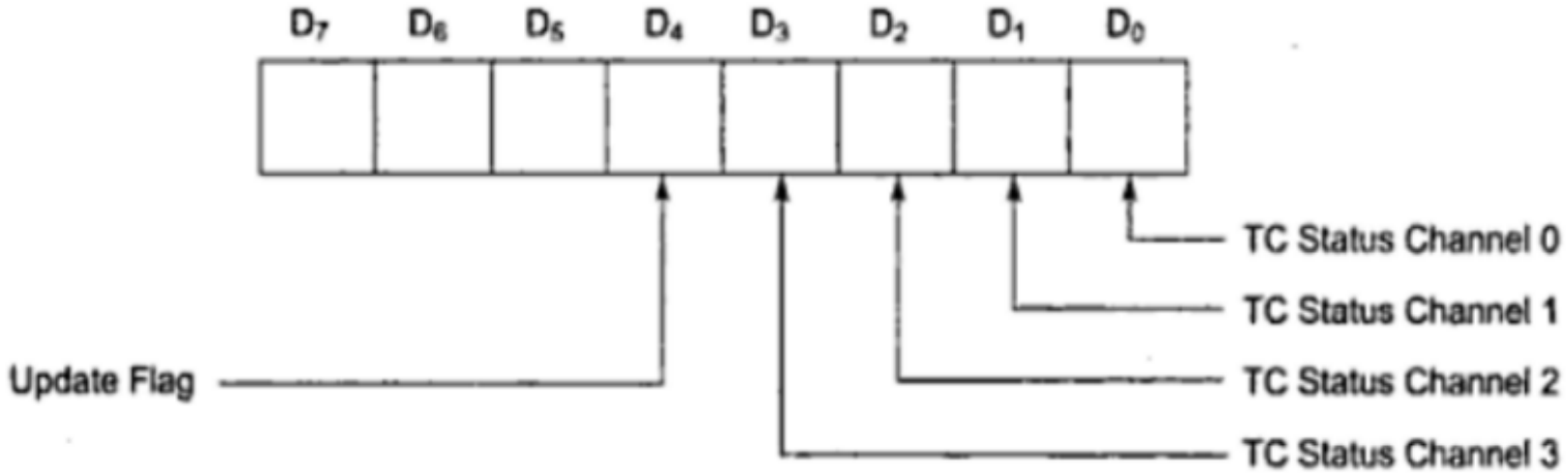
This register is programmed after initializing terminal count and DMA address registers



Programmable DMA controller : 8257

Control Logic Block :

Status Register : provides status of DMA channel. TC bits are set when TC signal is high for that channel.They remain set until status register is read or 8257 is reset



Programmable DMA controller : 8257

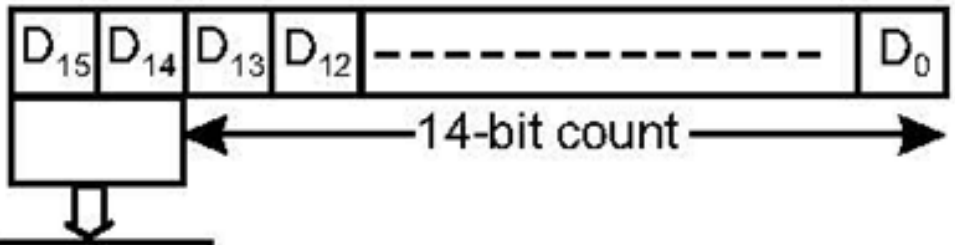
DMA CHANNELS:

DMA Address Register : 16 bit register used to hold starting address of memory. It is incremented after each DMA cycle. Memory address must be programmed before channels are enabled.

Terminal Count Register : 16 bit register divided into two fields; 14 bit of count and 2 bits of cycle control bits. The count value is decremented after every DMA cycle. The count of DMA cycles and type of cycle must be programmed before channel is enabled.

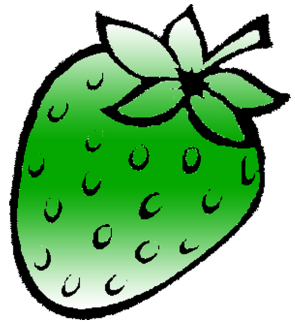
Programmable DMA controller : 8257

Terminal Count Register



Verify DMA cycle	0	0
Write DMA cycle	0	1
Read DMA cycle	1	0
Illegal	1	1

STRAWBERRY



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